Review of RC Circuits

EECS 373 Notes

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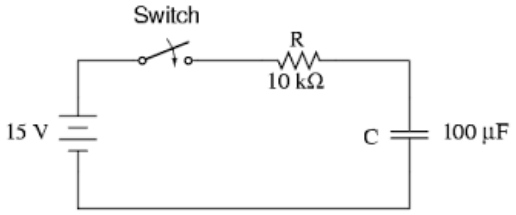
Resistor-capacitor (RC) circuits emerge in a variety of places in everyday embedded systems. This refresher provides several common examples that are, at their root, applications of RC circuits. We'll also see how to apply a few common patterns to solve these problems.

1. **Charging a capacitor through a resistor.** Consider the circuit shown below that includes battery (V_{bat} = 15 V), switch (that we will close at time t = 0), resistor R (10 kΩ) and capacitor C (100 μF). Assume that the capacitor is initially discharged (V_{cap} = 0 V). Once the switch is closed, how long does it take for the capacitor voltage, V_{cap}, to rise to 80% of V_{bat}?



Solution. The voltage, $V_{cap}(t)$, across an initially discharged capacitor, C, charged through a resistor, R, from a voltage source, V_{bat}, is described by the following equation (τ = RC):

$$V_{cap}(t) = V_{bat}\left(1 - e^{-t/\tau}\right)$$

rearranging, we have:

$$e^{-t/\tau} = \left(1 - \frac{V_{cap}(t)}{V_{bat}}\right)$$

$$-t/\tau = \ln\left(1 - \frac{V_{cap}(t)}{V_{bat}}\right)$$

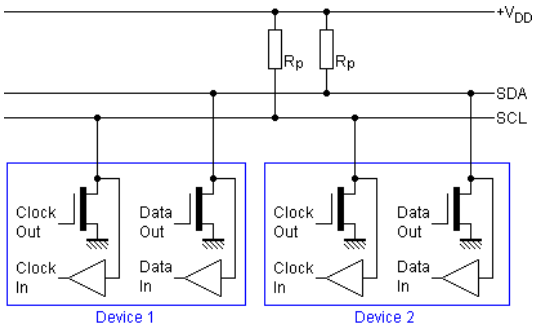
$$t = -\tau \ln\left(1 - \frac{V_{cap}(t)}{V_{bat}}\right)$$

replacing τ with RC = 10 kΩ ·100 μF = 1 s, $V_{cap}(t)$ = (80%)·(15 V) = 12 V, and V_{bat} = 15V:

$$t = -(1 \text{ sec}) \times \ln\left(1 - \frac{12}{15}\right) = -\ln 0.2 \text{ sec} = -(-1.61) \text{ sec} = 1.61 \text{ sec}$$

2. **I2C Rise Time.** The standard-mode I2C specification uses open-drain logic. Under this scheme, bus devices drive the SCL and SDA bus lines low (to 0 V) but rely on a shared, external pull-up resistor (typically 10 kΩ) to send a high bit (at 3.3V or 5V) by "pulling-up" the bus line. **How long** will a low-to-high transition take, after the SDA line has been at 0V for a long time, if low is 0 V, V_{DD} is 3 V, a "high" is 80% of V_{DD} (e.g. 2.4 V), the aggregate bus capacitance is 50 pF, and a 10 kΩ pull-up resistor is used?

Solution. Note that this problem is very similar to the first example. The only difference here is that the resistor is a 10 kΩ "pull-up" and the "capacitor" is the sum of all of the bus and gate capacitances (*i.e.* the aggregate input capacitance of the buffers shown below that are connected to SDA and SCL).



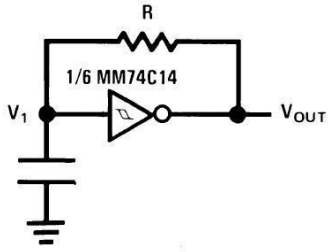
So, we simply use the same approach as before:

$$t = -\tau \ln\left(1 - \frac{80\% \times V_{DD}}{V_{DD}}\right)$$

replacing τ with RC = 10 kΩ ·50 pF = 0.5 µs, V_{DD} = 3 V:

$$t = -(0.5\ \mu s) \times \ln\left(1 - \frac{0.8}{1}\right) = -(0.5\ \mu s) \times \ln 0.2\ \text{sec} = -\ (0.5\ \mu s) \times (-1.61) = \ 0.8\ \mu s$$

3. **Clock Generation.** Assume you are designing a CMOS RC oscillator that must generate a 1 MHz clock (V_{OUT}) using the circuit shown below. Assume that V_{CC} is 5 V, that the 74C14's valid "high" input is ≥80% of V_{CC} and valid "low" input is ≤20% of V_{CC}, that it outputs 0 V for a "low" and 5 V for a "high," and that it has a negligible propagation delay. Find values for R and C that will result in the following circuit generating the desired output frequency.



Solution. The key to this problem is recognizing that when the inverter's output is driven low (when V_{OUT} = 0 V), the capacitor, C, is being discharged through the resistor, R. And, when the inverter's output is driven high (V_{OUT} = 5 V), the capacitor, C, is being charged through the resistor, R. We've already explored the equation that governs charging a capacitor through a resistor, but what about the equation that governs discharging a charged capacitor through a resistor? It's even simpler! Assuming that a capacitor, C, that was charged to an initial voltage, V_0, is discharged through a resistor, R, starting at time t = 0, the voltage across the capacitor, $V_{cap}(t)$, is given by:

$$V_{cap}(t) = \ V_0 \cdot e^{-t/\tau}$$

rearranging to solve for t:

$$t = -\tau \ln\left(\frac{V_{cap}(t)}{V_0}\right)$$

When power is first applied, the capacitor starts off discharged, so the input into the 74C14's is 0 V, and therefore it's output becomes 5 V. At this point, the capacitor, C, begins charging through resistor, R. This charging will continue until $V_{cap}(t)$ reaches 80% of V_{CC}, at which point the input to the 74C14 will reach the threshold for a "high" input, and the output will instantaneously switch to "low" and produce a 0 V output. This will cause the capacitor, C, to begin discharging from a voltage $V_{cap} = 80\% \cdot V_{CC} = 4$ V. Once V_{cap} reaches 20% of V_{CC}, the 74C14's output will again switch "high" and the capacitor will continue charging.

So, the question to answer is how long does it take for a capacitor, C, to discharge from 80% to 20% voltage and how long does it take for a capacitor to charge from 20% to 80% voltage? To answer the first (discharge) question, we can use:

$$t = -\tau \ln\left(\frac{V_{cap}(t)}{V_0}\right)$$

$$t = -\tau \ln\left(\frac{20\%}{80\%}\right) = -\tau(\ln(0.2) - \ln(0.8)) = 1.39\,\tau = 1.39 \cdot R \cdot C$$

And to answer the second (charge) question, we can either work through the following equation for the times that $V_{cap}(t)$ are at 20% and 80% of V_{CC}, and take their difference:

$$t = -\tau \ln\left(1 - \frac{V_{cap}(t)}{V_{CC}}\right)$$

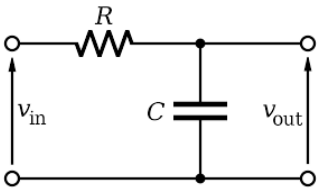
Alternately, we can recognize the symmetry in the fall and rise times, and be happy that we can just do the math once! Since t represents a ½ cycle of the 1 MHz clock (discharge), or 0.5 µs, we have:

$$0.5\ \mu s = 1.39 \cdot R \cdot C$$
$$R \cdot C = 0.36\ \mu s$$

Which would be satisfied by R = 1 Ω and C = 0.36 µF.

4. **Anti-Aliasing Filter.** Another use for an RC circuit is as a filter that limits the magnitude of spectral components of a signal above a given cutoff frequency. One common use of such a "low-pass filter" is as an anti-aliasing filter placed immediately before an ADC's input. Consider the RC-circuit shown below—a low-pass filter (LPF)—whose magnitude transfer function is given by:

$$\frac{|V_{out}|}{|V_{in}|} = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}}$$



where ω is the V_{in}'s frequency is radians (and where $\omega = 2\pi f$, and f is the frequency in Hz). If we would like this filter to attenuate the input, V_{in}, by 3 dB (so that $\frac{|V_{out}|}{|V_{in}|} = \frac{1}{\sqrt{2}}$) at 30 Hz, and we are given a capacitor, C, which has a value of 0.1 μF, what value should we choose for the resistor, R?

Solution. Notice that when $\frac{|V_{out}|}{|V_{in}|} = \frac{1}{\sqrt{2}}$, the expression $\sqrt{1 + \omega^2 R^2 C^2}$ must be equal to $\sqrt{2} = \sqrt{1+1}$, which means that $\omega^2 R^2 C^2 = 1$ and $\omega RC = 1$. Now, solving for R, we have:

$$R = \frac{1}{\omega C} = \frac{1}{2\pi f C} = \frac{1}{2 \cdot \pi \cdot 30 \cdot 1 \times 10^{-7}} = 53 \text{ k}\Omega$$