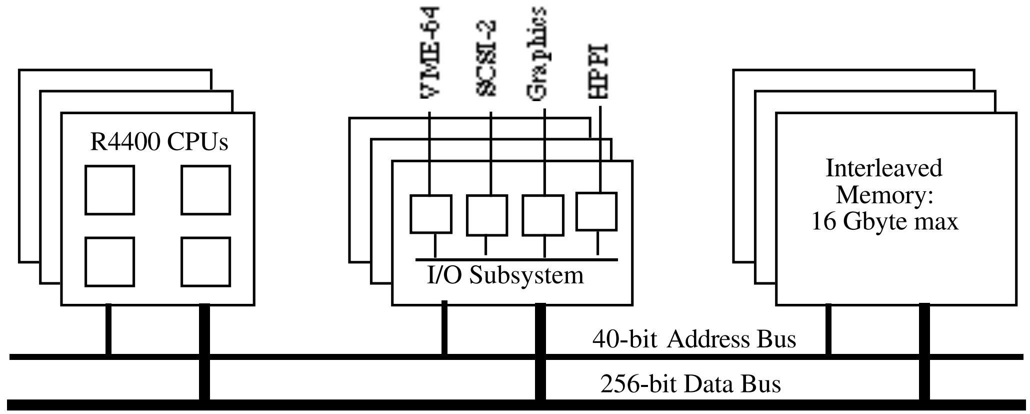
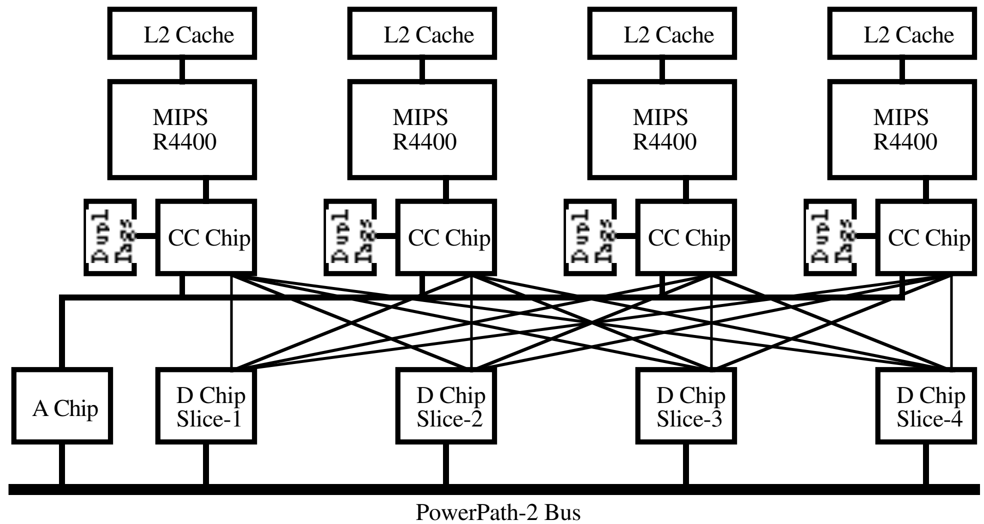
Parallel Machine Block Diagrams

SGI Challenge

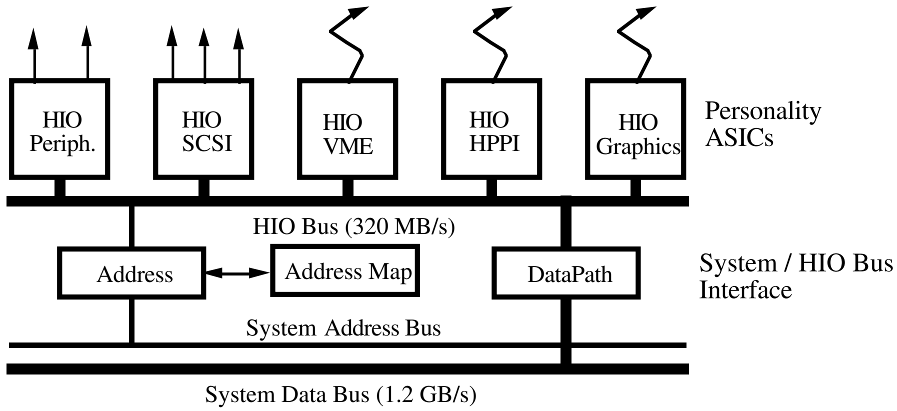


- 36 MIPS R4400 (peak 2.7 GFLOPS, 4 per board) or 18 MIPS R8000 (peak 5.4 GFLOPS, 2 per board)
- 8-way interleaved memory (upto 16 GB)
- 4 I/O busses of 320 MB/s each
- 1.2 GB/s bus @ 47.6 MHz, 16 slots, 329 signals
- 128 Bytes lines (1 + 4 cycles)
- Split-transaction with upto 8 outstanding reads
  - **all transactions take five cycles**
  - **parallel distributed arbitration**

SGI Challenge: Board Design

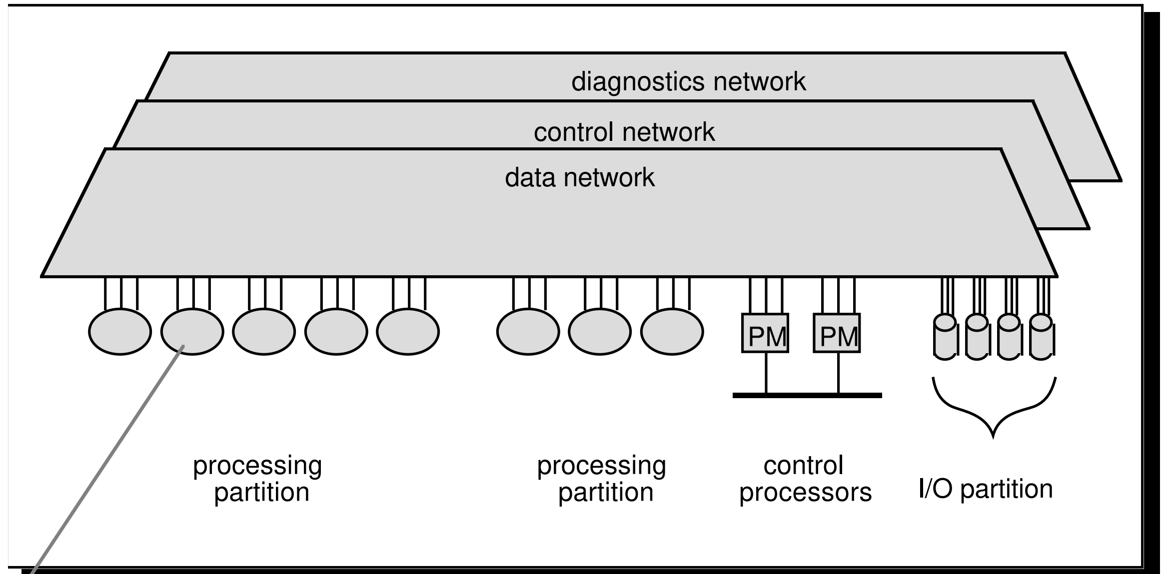


SGI Challenge: I/O Subsystem

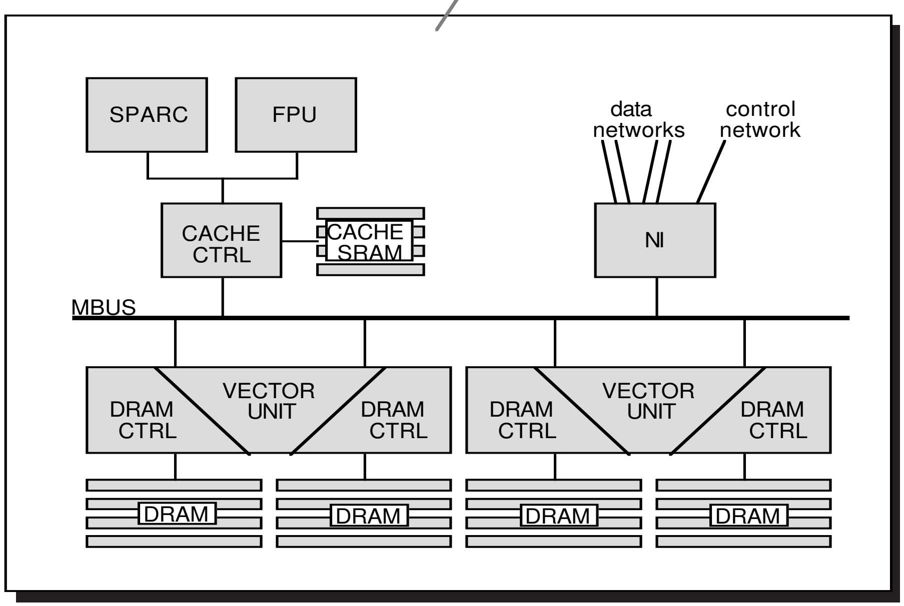


- HIO
  - **64-bit multiplexed address / data**
  - **split-read, upto 4 per device**
  - **pipelined, centralized arbitration**
  - **several transaction lengths**
  - **address remapping**
- I/O board acts like a processor to memory system

CM-5

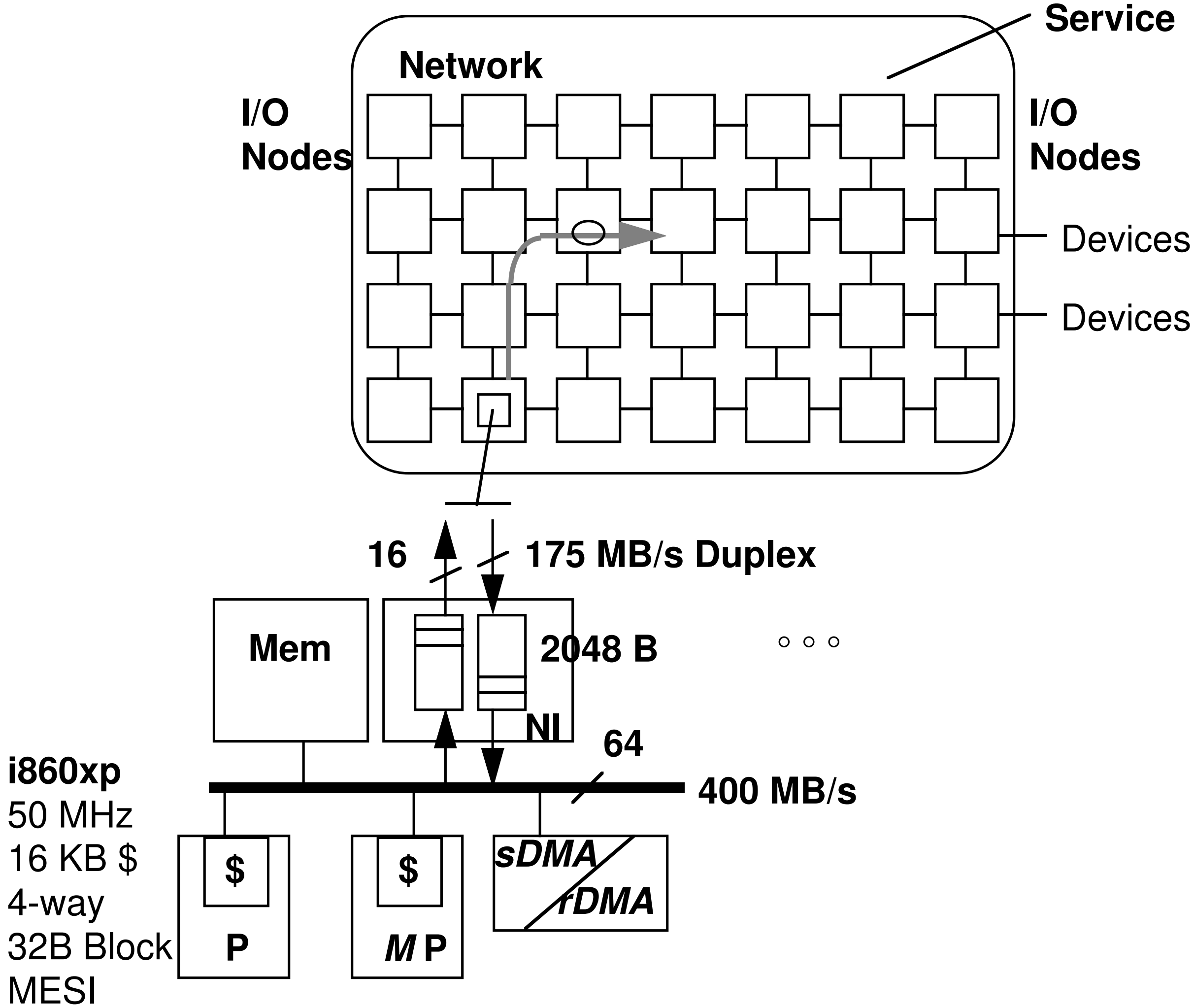


diagnostics network
control network
data network
PM
PM
processing partition
processing partition
control processors
I/O partition

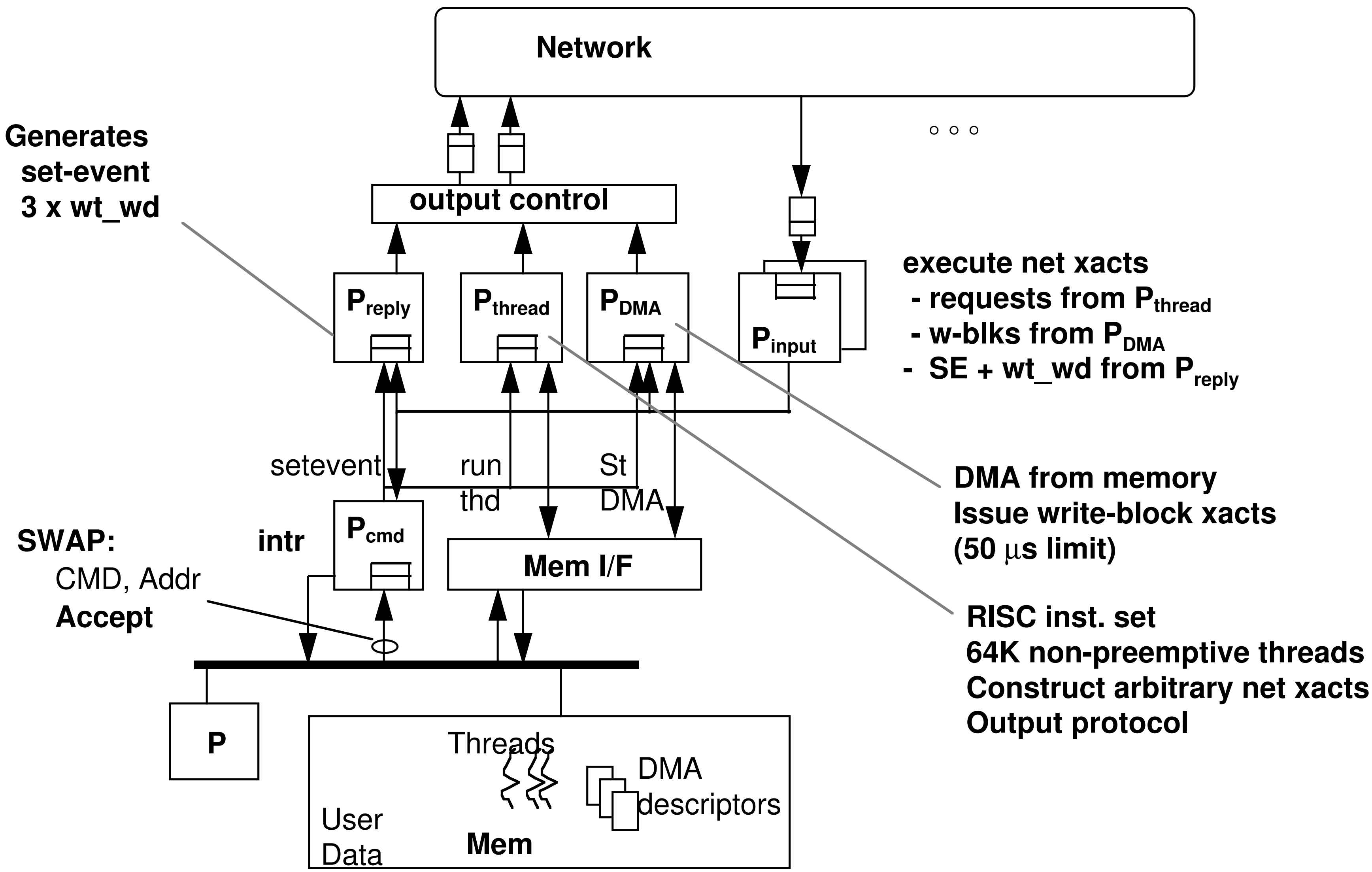


SPARC
FPU
CACHE CTRL
CACHE SRAM
data networks
control network
NI
MBUS
DRAM CTRL
VECTOR UNIT
DRAM CTRL
DRAM CTRL
VECTOR UNIT
DRAM CTRL
DRAM
DRAM
DRAM
DRAM

Intel Paragon

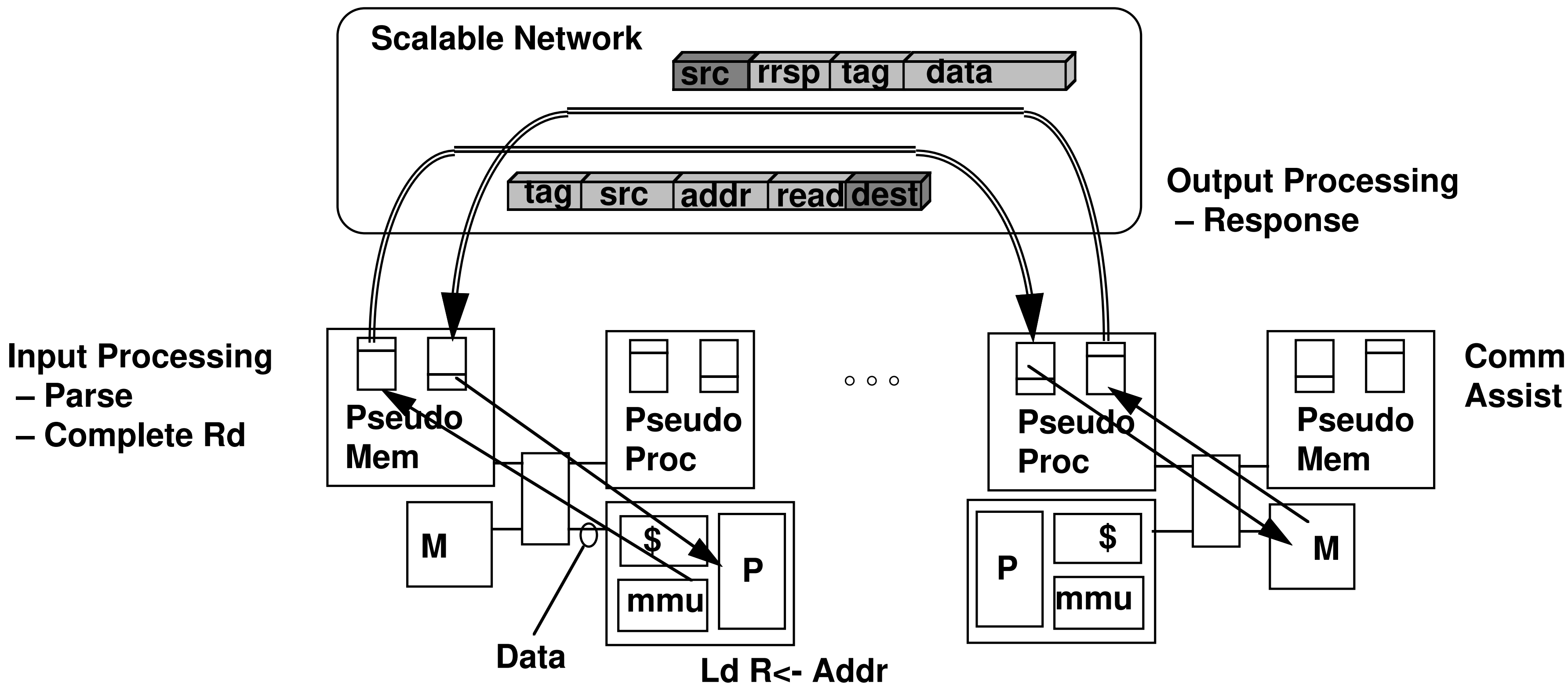


Meiko CS-2

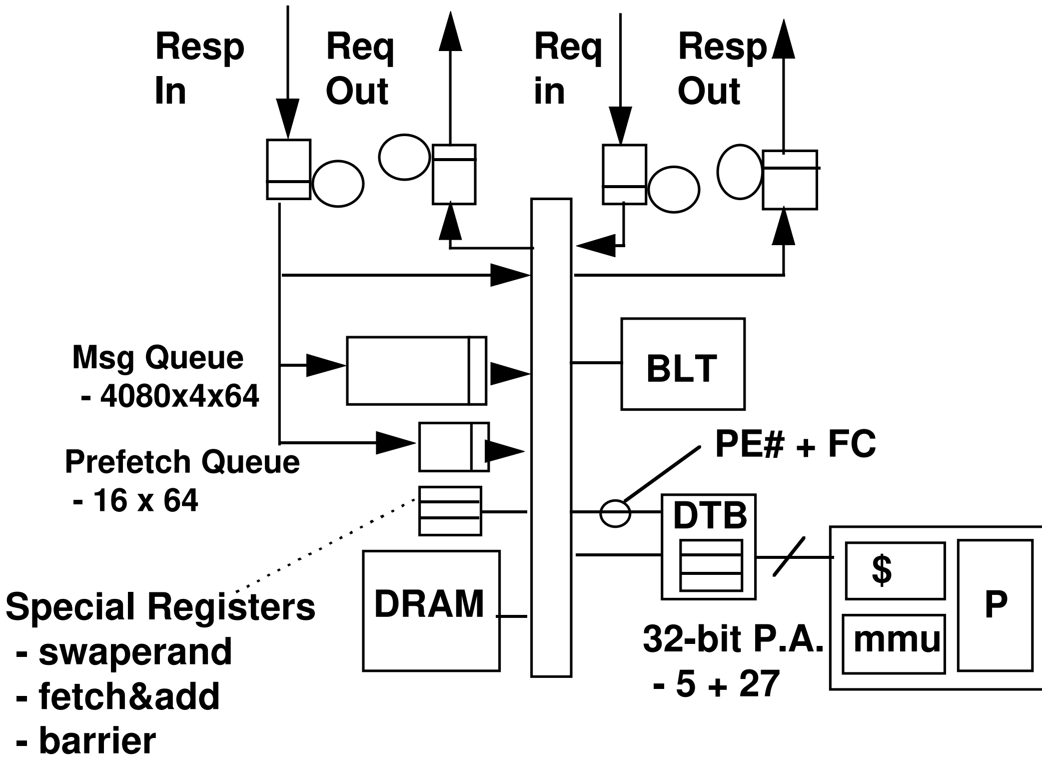


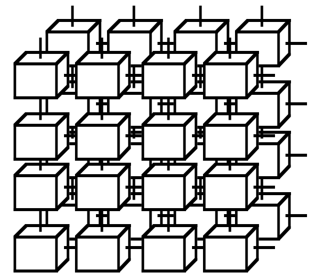
Network
Generates
set-event
3 x wt_wd
output control
P_{reply}
P_{thread}
P_{DMA}
P_{input}
execute net xacts
- requests from P_{thread}
- w-blks from P_{DMA}
- SE + wt_wd from P_{reply}
setevent
run
thd
St
DMA
DMA from memory
Issue write-block xacts
(50 μs limit)
SWAP:
CMD, Addr
Accept
intr
P_{cmd}
Mem I/F
RISC inst. set
64K non-preemptive threads
Construct arbitrary net xacts
Output protocol
P
Threads
DMA
descriptors
User
Data
Mem

Shared Physical Address



Cray T3D





3D Torus of Pair of PEs
- share net & BLT
- upto 2048
- 64 MB each

150 MHz Dec Alpha (64-bit)
8 KB Inst + 8 KB Data
43-bit Virtual Address
32 & 64 bit mem + byte operations
Non-blocking stores + mem-barrier
Prefetch
Load-lock, Store Conditional