Correspondence

A Class of Odd-Weight-Column SEC-DED-S*b*ED Codes for Memory System Applications

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Abstract — **Error correcting codes are widely used in memory systems to increase reliability. Especially in a memory system that uses byte-organized memory chips, which each contain b (>1) output bits, a single chip failure is likely to affect many bits within a byte. Single-bit error correcting–double bit error detecting–single b-bit byte error detecting codes (SEC-DED-SbED codes) are suitable for increasing the reliability of memory system.**

This correspondence presents a new class of odd-weight-column SEC-DED-SbED codes for $b = 4$. The code length is $2^{r-1} - 2^{\lceil r/2 \rceil}$, where r is the number of check bits and $\lceil\ \rceil$ denotes the ceiling or next largest integer. The proposed SEC-DED-S4ED codes are the best-known codes.

Index Terms — **Byte-organized memory chips, error-correcting codes, LSI implementation, reliability, single-bit error correcting–double-bit error detecting–single-b-bit byte error detecting codes (SEC-DED-SbED codes).**

I. Introduction

Error correcting codes are widely used in memory systems to increase reliability [1], [6]. As LSI technology moves towards higher levels of integration, byte-organized memory chips, which each contain b (≥ 2) output bits, have become the general practice. However, for such byte-organized memory chips, a single chip failure is likely to affect many bits within a byte.

Many codes have been proposed for correction and/or detection of several classes of potential failures in memory systems using byte-organized memory chips. In particular, single-bit error correcting–double-bit error detecting–single-b-bit byte error detecting codes (SEC-DED-SbED codes), for correcting single-bit errors and simultaneously detecting double-bit errors and single-b-bit byte errors, can be effectively and economically applied to this kind of memory system to increase reliability. Certain known codes which correct both bit and byte errors [7], [8] can be applied; however, these codes require greater redundancy than SEC-DED-SbED codes do.

Single-bit error correcting–single-b-bit byte error detecting (SEC-SbED) codes have been proposed by Bossen *et al.* [2], and Reddy [3] extended the protection provided by Bossen, Chang, and Chen through constructing similar SEC-SbED codes in which the class of detectable errors was enlarged to include double errors. In addition, Fujiwara [4], Kaneda and Fujiwara [5], Chen [11], and Dunning and Varanasi [12] all have proposed SEC-DED-SbED codes. Specifically, the present author proposed minimum-weight rotational SEC-DED-SbED codes, where code length is $b(b + 2)$ for the number of check bits $(r) = b + 2$ [13].

In this correspondence, a new class of odd-weight-column SEC-DED-S4ED codes is proposed. The proposed codes are best-known codes for $b = 4$.

II. New Class of Odd-Weight-Column SEC-DED-S4ED Code

The following theorem gives SEC-DED-SbED codes when $b = 4$ and $r =$ an even positive number.

Manuscript received February 9, 1982; revised February 20, 1984.

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Theorem: Let r be an arbitrary but positive even number ($r > 3$). The following Steps 1–4 give SEC-DED-S4ED codes, where the code length is $2^{r-1} - 2^{r/2}$ bits.

Step 1: Let g denote a column vector having $r/2$ binary elements. Vector g is arbitrary, but $g =$ all "1" is advisable to reduce the H matrix weight.

Step 2: Let f_q denote a column vector having $r/2$ binary elements. The weight of f_q must be even for an odd-weight g, and must be odd for an even-weight g. The number of f_q's is $2^{(r/2-1)}$ $(q = 0, 1 \cdots 2^{(r/2-1)} - 1)$.

Step 3: Two column vectors f_i and f_j are selected arbitrarily from the f_q's where $0 \leq i \leq 2^{(r/2-1)} - 1, 0 \leq j \leq 2^{(r/2-1)} - 1$, and $i \neq j$. Using f_i and f_j, the following r by 4 matrix, h_{ij}, is defined. (In (1), "+" represents the modulo-2 sum of the column vectors.)

$$h_{ij} = \left[\begin{array}{c|c|c|c} g + f_i + f_j & g + f_i + f_j & f_i & f_j \\ f_i & f_j & g + f_i + f_j & g + f_i + f_j \end{array}\right]. \tag{1}$$

Step 4: The H matrix for the proposed SEC-DED-SbED codes can be defined as follows, using this h_{ij}:

$$H = [h_{01}, h_{02}, h_{03}, \cdots h_{ij} \cdots]. \tag{2}$$

Proof: Obviously, the column vectors for (2) are odd weight. Now, let us assume that f_i is odd weight. In this case, g must be even weight. Even if f_i is even weight, the proof is the same, as will be shown.

1) Proof of single error correcting capability: The weight of f_i is odd and the weight $g + f_i + f_j$ is even. Thus, the following equations should be satisfied to show the nonuniqueness of the column vectors:

$$f_i = f_i'$$

$$g + f_i + f_j = g + f_i' + f_j'$$

where if $f_i = f_i'$ then f_j must not be equal to f_j' from the definition in the theorem. However, we can derive $f_i = f_i'$ and $f_j = f_j'$ from these equations, which is absurd. Thus, the column vectors for (2) are distinct. Consequently, the codes in (2) are SEC-DED codes.

2) Proof of single-4-bit byte error detecting: Double-bit errors within each byte can be detected through DED capability. Let us verify this error detection capability for triple-bit errors and four-bit error within a byte.

a) Triple-bit errors within a byte: For each byte of (2), let us chose an arbitrary three column vector from that byte and sum them. The resultant column vector pattern is a syndrome for a triple-bit error. It can easily be shown that either lower-half $r/2$ bits or upper-half $r/2$ bits in the syndrome are equal to g. Note (2) again. From the definition in the theorem, f_i is not equal to f_j; therefore, $g + f_i + f_j$ cannot be equal to g. As a consequence, triple-bit errors within each byte can be detected.

b) Four-bit errors within a byte: For each byte of (2), sum the four column vectors. Obviously, the resultant column vector is even weight and is not equal to the all "0" vector. Thus, a four-bit error within each byte can be detected.

Note that the number of f_q's is $2^{(r/2-1)}$. In addition, the number of h_{ij}'s is the combination number with selection of two elements from $2^{(r/2-1)}$ elements. The code length can be easily obtained. Q.E.D.

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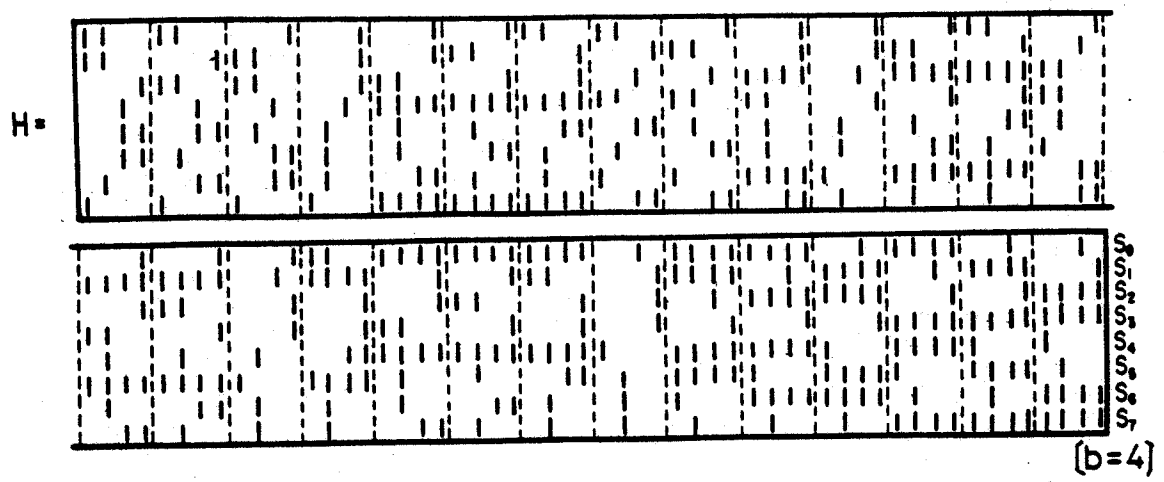

Fig. 1. (112, 108) minimum-weight SEC–DED–S4ED code.

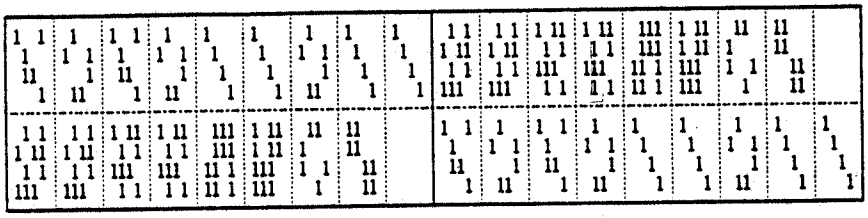

Fig. 2. (72, 64) 2-rotational SEC–DED–S4ED code.

So as to show this process concretely for $b = 4$ and $r = 8$, let g be an all "1" vector

$$g = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix}. \tag{3}$$

This g is even weight; therefore, f_q must be odd weight. There are eight f_q's in this case. The f_q's are

$$f_q = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}, \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 1 \\ 0 \\ 1 \end{bmatrix}, \begin{bmatrix} 1 \\ 0 \\ 1 \\ 1 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \\ 1 \\ 1 \end{bmatrix}. \tag{4}$$

From these f_q's two columns are chosen, and the $h_{i,j}$ matrix is constructed. There are 28 $h_{i,j}$'s in this case. For instance, h_{01} and h_{02} are

$$h_{01} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}, \quad h_{02} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}. \tag{5}$$

The complete H matrix for $b = 4$ and $r = 8$ is given in Fig. 1. We can easily obtain the shortened $r/2$-rotational SEC–DED–S4ED codes from the proposed codes. Fig. 2 shows the 2-rotational odd-weight-column (72, 64) SEC–DED–S4ED code shortened and converted from the Fig. 1 code. In this case, check columns (weight = 1 columns) are concentrated into two bytes using vector operations among row vectors.

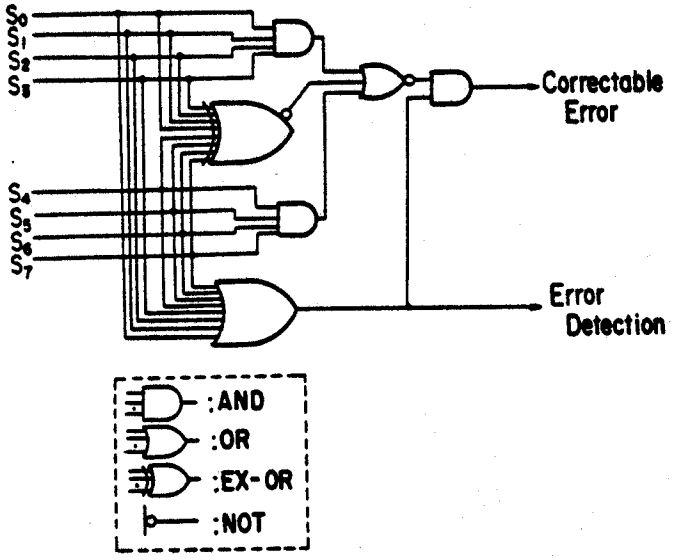

Fig. 3. Error detecting circuit for Fig. 1 code.

For the SEC–DED–SbED codes given by the theorem, as was mentioned in the proof, either the upper $r/2$ bits or lower $r/2$ bits of the syndrome for triple-bit errors within a byte are equal to g. Taking advantage of this property, it is possible to systematically construct error detecting circuitry with a small number of gates. Fig. 3 shows the error detecting circuitry for the Fig. 1 code.

The number of check bits is an even number for the proposed code. If an odd number of check bits is required, construction A in [11] can be applied to the proposed codes. Thus, the code length of the proposed code is $2^{r-1} - 2^{\lceil r/2 \rceil}$ bits, where $\lceil\ \rceil$ denotes the ceiling or next largest integer.

III. Conclusion

This correspondence has proposed a new class of odd-weight-column SEC–DED–S4ED codes. The code length is $2^{r-1} - 2^{\lceil r/2 \rceil}$ bit, where b is the byte length, r is the number of check bits, and $\lceil\ \rceil$ is the ceiling or next largest integer. The proposed codes are best-known codes for $b = 4$.

The proposed odd-weight-column SEC–DED–S4ED codes can be practically and effectively applied to main storage systems using byte-organized memory chips.

Acknowledgment

The author thanks Dr. C. L. Chen for his private communication concerning [11]. In addition, the author thanks Prof. S. M. Reddy for his communications.

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