Place your name on **all** of the pages containing questions.
There should be a total of **8 pages** in this exam, including the figure at the end.

Note: For this exam, 1 MB = 2^{20} bytes.

1. "Double your Pleasure"	
2. "Queueing the Network"	
3. "RAIDers and RAINers"	
4. "Cleaning up the States"	
Total	

1. "Double your Pleasure"

a) Give one reason why speedup is not a good way to measure the performance of a multiprocessor.

b) Give a situation where a program is **more than** twice as fast when you double the number of processors in a multiprocessor.

1. “Double your Pleasure” (cont’d)

c) What is the “fourth C” for multiprocessors?

How does the fourth C change as you increase block size in a shared memory multiprocessor? Why?

d) Suppose a parallel machine with 100 processors can function in just two modes: parallel (in which all processors are used) and serial (in which only one processor at a time is doing useful work). What is the maximum percentage of time that a parallel application can spend in serial mode for a speedup of 80 compared to the sequential version?

2. “Queueing the Network”

Measurements of a network gateway show that packets arrive at 200 packets per second and that the gateway forwards them in about 2 ms. Assume that the interarrival times between messages are exponentially distributed and the system is in equilibrium. From this information, answer these questions about the gateway:

a) What is the utilization of the gateway?

b) What is the mean number of packets in the gateway?

c) What is the mean time spent in the gateway?

2. “Queueing the Network” (cont’d)

d) For an M/M/1 queue, the probability of find n or more tasks in the system is Utilization^n. What is the chance of an overflow of the FIFO if it can hold 10 messages?

e) For a larger number of packets, if the probability of any one packet finding the queue full is one per million, then on average only one packet will be lost per million processed. How big must the gateway FIFO be to have packet loss due to FIFO overflow to be less than one packet per million?

f) Gateway manufacturers limit FIFO size to keep costs down. How would you ensure delivery given packet loss due to FIFO overflow?

3. “RAIDers and RAINers”

a) List at least 2 advantages of a disk array versus a single large disk.

b) Suppose that the a disk has a measured average seek time of 5 ms, rotates at 6000 RPM, the sector size is 0.001 MB, and the transfer rate is 10 MB/second. Assume that you have 4 of these disks. Fill in the tables below with the number of I/Os per second for RAID 1 (mirroring) and RAID 5 (rotated parity) separately for 100% reads and 100% writes using transfer sizes of 0.001 MB and 1.0 MB. **Show your work.**

Table 1: I/Os per second for RAID 1

	Reads	Writes
Size= 0.001 MB		
Size= 1.000 MB		

Table 2: I/Os per second for RAID 5

	Reads	Writes
Size= 0.001 MB		
Size= 1.000 MB		

3. “RAIDers and RAINers” (cont’d)

c) We have seen the advantages of building large storage system from several inexpensive small disks. What are the pros and cons of creating a single fast local area network (LAN) from several slow, inexpensive LANs?

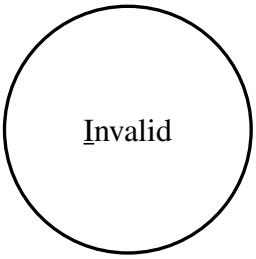
Pros:

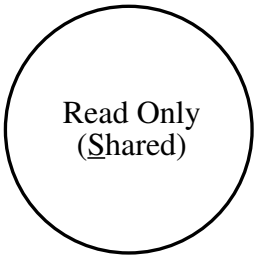
Cons:

4. “Cleaning up the States”

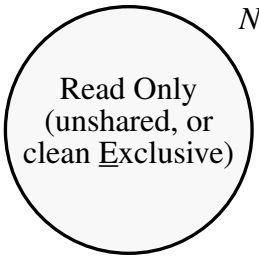
The popular MESI (Modified, Exclusive, Shared, Invalid) protocol has a clean exclusive state not found in the example in the book. It is predicated on being able to distinguish a read miss that will retrieve a block in which the requesting processor will have the only copy (exclusive) vs. not having the only copy (shared). Assume we have a write back protocol as in the book. The attached page shows the state diagram for the 3 state protocol given in the book.

Only show the new arcs needed for this 4 state protocol; that is, assume that any arcs that are identical to the 3 state protocol, shown on the next page, are already there. **Be sure to label each arc with the LABEL(S) FROM THE TABLES BELOW corresponding to the CPU stimulus(i), CPU action(s) on the bus, and/or bus operation(s) as appropriate**.





New State



Label	CPU stimulus causing transition
CRH	CPU read hit
CRMs	CPU read miss (shared)
CRMx	CPU read miss (exclusive)
CWH	CPU write hit
CWM	CPU write miss

Label	CPU action on bus
PRM	place CPU read miss on bus
PWM	place CPU write miss on bus
WB	write back cache block

Label	Operation on bus causing transition
BRM	read miss for this block
BWM	write miss for this block