Supporting Systolic and Memory Communication in iWarp

(Borkar et al. 1990)

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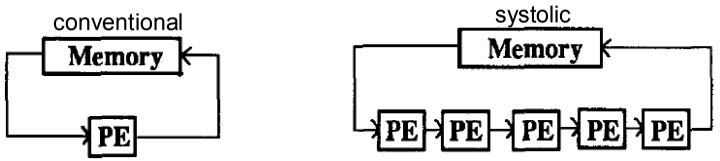
Fine-grain parallelism: how?

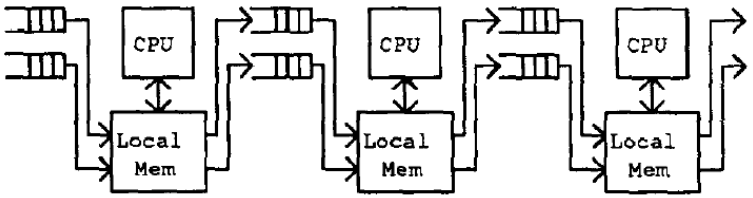
- Borrow ideas from systolic arrays!
- Systolic arrays: a multiprocessor architecture



- Replication of PEs, not unsimilar to SIMD
- Fine-grain communication, pipeline-style
- Requires special algorithms, special-purpose hardware
- The idea: direct PE-to-PE communication (inexpensive?!)

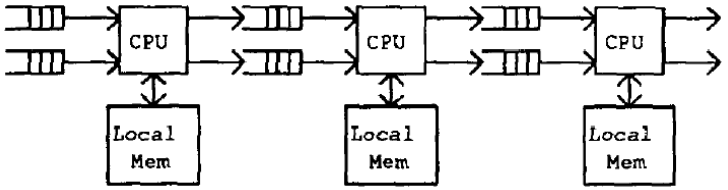
Traditional (memory) communication

- Decoupled computation/communication
- Legacy of networkless stations?



Systolic communication

- Do not get memory involved
- Requires special CPU support

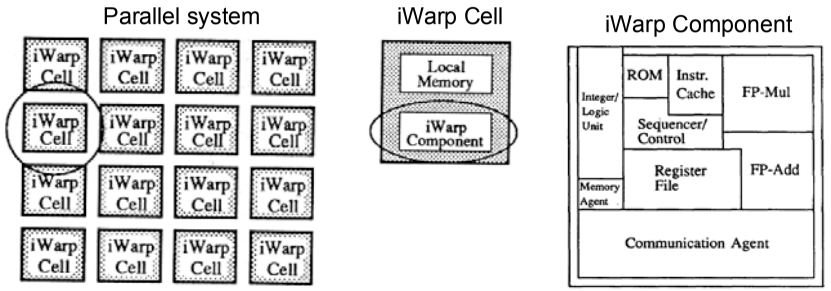


iWarp system

- Both systolic and memory communication
  - Systolic communication = performance
  - Memory communication = general purpose
- Parallel with vector processors:
  - They usually have both vector and scalar units
  - And get best of both
- Will this idea be similarly successful?
  - Was manufactured by Intel
  - But not anymore

Outline of the base system

- 8x8 mesh or torus (can be scaled to 32x32)
- Distributed memory
- Custom network, custom nodes
- Communication layer implemented in hardware
  - On the same chip with CPU



Program access to communication

- Network input/output queues are accessible via CPU registers (“gates”)
- Reading from gate pops data from the input queue, writing – inserts into the output queue
- One instruction can involve up to 4 communication operations! (e.g. D=C+A*B)
- Reading = polling (vs. interrupts in MDP)
- Stall if input queue is empty or if output queue is full
- Option to spill queues to memory

Bandwidth reservation

- Logical channels (aka virtual channels)
  - Multiplexed over physical buses (roundrobin)
  - Idle and blocked virtual channels don’t participate
- Two routing modes
  - Route messages individually
    - Logical channels are acquired and released for transporting each message
  - Route via an established connection (pathway)
    - Acquire a sequence of logical channels first
    - Use these resources for transport