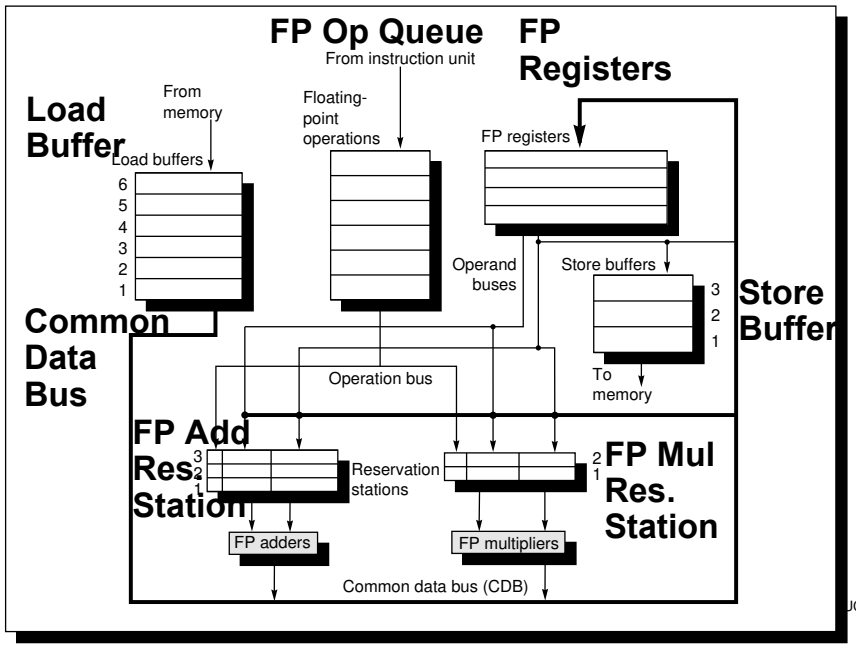
# Tomasulo Organization



# Three Stages of Tomasulo Algorithm

1. Issue—get instruction from FP Op Queue

   If reservation station free (no structural hazard),
   control issues instr & sends operands (renames registers).

2. Execution—operate on operands (EX)

   When both operands ready then execute;
   if not ready, watch Common Data Bus for result

3. Write result—finish execution (WB)

   Write on Common Data Bus to all awaiting units;
   mark reservation station available

- Normal data bus: data + destination ("go to" bus)
- Common data bus: data + source ("come from" bus)
  - 64 bits of data + 4 bits of Functional Unit source address
  - Write if matches expected Functional Unit (produces result)
  - Does the broadcast

# Tomasulo Example Cycle 0

| Instruction status | | | | *Execution* | *Write* | | | |
|---|---|---|---|---|---|---|---|---|
| Instruction | | *j* | *k* | *Issue* | *complete* | *Result* | | Busy Address |
| LD | F6 | 34+ | R2 | | | | Load1 | No |
| LD | F2 | 45+ | R3 | | | | Load2 | No |
| | F0 | F2 | F4 | | | | Load3 | No |
| SUBD | F8 | F6 | F2 | | | | | |
| DIVD | F10 | F0 | F6 | | | | | |
| ADDD | F6 | F8 | F2 | | | | | |

| Reservation Stations | | | *S1* | *S2* | *RS for j* | *RS for k* |
|---|---|---|---|---|---|---|
| *Name* | | *Op* | *Vj* | *Vk* | *Qj* | *Qk* |
| 0 | Add1 | No | | | | |
| 0 | Add2 | No | | | | |
| 0 | Add3 | No | | | | |
| 0 | Mult1 | No | | | | |
| 0 | Mult2 | No | | | | |

| Register result status | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Clock | *F0* | *F2* | *F4* | *F6* | *F8* | *F10* | *F12* | ... | *F30* |
| **0** *FU* | | | | | | | | | |

# Loop Example Cycle 0

Instruction status

| | | j | k | iteration | Issue | Write Result | | Busy | Address | |
|---|---|---|---|---|---|---|---|---|---|---|
| LD | F0 | 0 | R1 | 1 | | | Load1 | No | | |
| | F4 | F0 | F2 | 1 | | | Load2 | No | | |
| SD | F4 | 0 | R1 | 1 | | | Load3 | No | | Qi |
| LD | F0 | 0 | R1 | 2 | | | Store1 | No | | |
| | F4 | F0 | F2 | 2 | | | Store2 | No | | |
| SD | F4 | 0 | R1 | 2 | | | Store3 | No | | |

Reservation Stations

| | Name | Op | S1 Vj | S2 Vk | Qj | Qk | RS for k |
|---|---|---|---|---|---|---|---|
| 0 | Add1 | No | | | | | |
| 0 | Add2 | No | | | | | |
| 0 | Add3 | No | | | | | |
| 0 | Mult1 | No | | | | | |
| 0 | Mult2 | No | | | | | |

Code:

```
LD    F0   0  R1
      F4   F0 F2
SD    F4   0  R1
SUBI  R1   R1 # 8
BNEZ  R1   Loop
```

Register result status

| Clock | R1 | F0 | F2 | F4 | F6 | F8 | F12 ... |
|---|---|---|---|---|---|---|---|
| 0 | 80 | Qi | | | | | |