University of California, Berkeley
College of Engineering
Computer Science Division — EECS

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Prerequisite Quiz Solutions
CS252 Graduate Computer Architecture

You are allowed to use a calculator and one 8.5" x 11" double-sided page of notes. Show your work on all problems. Good luck!

Question 1

Below is a series of memory read references sent to a cache. The cache has 32 bytes total with 2-byte blocks, is 2-way set associative, and uses a least recently used replacement policy. Assume the cache is initially empty.

Classify each memory reference as a hit or a miss. Identify each cache miss as a Compulsory or a Conflict miss. One example is shown below. Blank working space is available on the next page.

$$\frac{32\text{ B}}{2\text{ B/block}} = 16\text{ blocks}$$
$$\frac{16\text{ blocks}}{2\text{ sets/block}} = 8\text{ sets}$$

So, we have 8 sets.

Byte Address	Hit/Miss?	Miss Type
1	Miss	Compulsory
6	Miss	Compulsory
30	Miss	Compulsory
17	Miss	Compulsory
7	Hit	N/A
0	Hit	N/A
18	Miss	Compulsory
32	Miss	Compulsory
17	Miss	Conflict
0	Miss	Conflict

Index	Set 0	Set 1
0	~~0 1~~ 16 17	~~16 17~~ ~~32 33~~ 0 1
1	18 19	
2		
3	6 7	
4		
5		
6		
7	30 31	

Note that block (32, 33) knocks out block (16, 17) because block (0, 1) is more recently used. Also note that byte 17 and byte 18 are in different blocks.

Question 2

The code below is going to be run on a 5-stage MIPS pipeline with a single branch delay slot. Identify all the data hazards that can be solved with forwarding to prevent any stalls, and all the data hazards that will cause a stall. Assume that a register can be written and read on the same cycle without forwarding, and this will not cause a stall.

```
0              li     $2, 5          # Number of iterations
4       lp:    shli   $4, $2, 2      # Translate to word address
8              lw     $5, 100($4)    # Load a new word
12             addi   $5, 4          # Add value
16             beqz   $2, exit       # Check if we're done
20             sw     $5, 100($4)    # (Delay slot) Store new value
24             b      lp             # Next iteration
28             addi   $2, -1         # (Delay slot) Advance pointer
32      exit:
36             addi   $10, 0         # Extra example instruction
40             addi   $11, $10, 0    # Extra example instruction
```

Complete the table below. "Source Instr" refers to the instruction that is *writing* to the register. "Dest Instr" refers to the instruction that is *reading* from the register. For both the "Source Instr" and "Dest Instr", write the number to the left of each instruction above. "Register" refers to the register involved in the hazard. Write "yes" or "no" in the "Stall even if forward?" column to indicate if the hazard will cause a stall even if forwarding is used. One example is shown below.

Source Instr	Dest Instr	Register	Stall even if forward?
36	40	10	No
0	4	2	No
4	8	4	No
8	12	5	Yes
12	20	5	No
28	4	2	No

Question 3

A system has 32 bit virtual addresses, 30 bit physical addresses, and 4 kilobyte pages.

a) Label the field names and bit boundaries of a virtual address and a physical address on this system.

bit position:	31 — 12	11 — 0
Virtual Address:	Virtual Page Number	Page Offset

bit position:	29 — 12	11 — 0
Physical Address:	Physical Page Number	Page Offset

b) Calculate the size of the page table on this system, if all virtual pages are in use. Assume that status bits (such as valid, protection, dirty, or use bits) take a total of 14 bits per entry in the table. Disk addresses are not stored in the page table.

First, calculate the size of each entry:

Size of entry = size of status bits + size of physical page number

= 14 bits + 28 bits

= 32 bits = 4 bytes = 2^2bytes

Next, calculate the number of entries:

Number of entries = number of virtual page

$= 2^{(\text{number of virtual page number bits})}$

$= 2^{20}$

The total size of the table is then the product:

Total size = Size of entry $*$ Number of entries

$= 2^2$ bytes $* \, 2^{20}$ bytes

$= 2^{22}$ bytes

= 4 megabytes