CS61C - Machine Structures

Lecture 10 - Floating Point, Part II and Miscellaneous

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Review

[°]Floating Point numbers approximate values that we want to use.

- ^o IEEE 754 Floating Point Standard is most widely accepted attempt to standardize interpretation of such numbers (\$1T)
- °New MIPS registers(\$f0-\$f31), instruct.:
- Single Precision (32 bits, 2x10⁻³⁸... 2x10³⁸): add.s, sub.s, mul.s, div.s
- Double Precision (64 bits, 2x10⁻³⁰⁸...2x10³⁰⁸): add.d, sub.d, mul.d, div.d

[°]Type is not associated with data, bits have no meaning unless given in context

Overview

- ^o Special Floating Point Numbers: NaN, Denorms
- ° IEEE Rounding modes
- ^o Floating Point fallacies, hacks
- ° Catchup topics:
 - · Representation of jump, jump and link
 - Reverse time travel:
 - MIPS machine language -> MIPS assembly language
 - -> C code
 - l spinel, shift instructions (time r
 - Logical, shift instructions (time permiting)

MIPS Floating Point Architecture (1/2)

- ° 1990 Solution: Make a completely separate chip that handles only FP.
- ^oCoprocessor 1: FP chip
 - contains 32 32-bit registers: \$f0, \$f1, ...
 most registers specified in .s and .d
 - instruction refer to this set
 - separate load and store: lwc1 and swc1
 ("load word coprocessor 1", "store ...")
 - Double Precision: by convention, even/odd pair contain one DP FP number: \$f0/\$f1, \$f2/\$f3,..., \$f30/\$f31

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^o Appendix pages A-70 to A-74 contain many, many more FP operations.



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| Special Numl ° What have v (Single Pred | bers (cont'd) we defined so cision)? | far? | _ |
|---|--|---------------|---|
| Exponent | Significand | Object | |
| 0 | 0 | 0 | |
| 0 | <u>nonzero</u> | <u>???</u> | |
| 1-254 | anything | +/- fl. pt. # | |
| 255 | 0 | +/- infinity | |
| 255 | nonzero | NaN | |
| | | | |
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Round to Even

^o Round like you learned in grade school

[°] Except if the value is right on the borderline, in which case we round to the nearest EVEN number

•2.5 -> 2

•3.5 -> 4

° Insures fairness on calculation

• This way, half the time we round up on tie, the other half time we round down

Ask statistics majors

° Default C rounding mode; only Java mode























| Decoding Example (4/6) | | | | |
|--|--------------------------------------|--|--|--|
| ° MIPS Assembly (Part 1): | | | | |
| $\begin{array}{c} 0 \times 004 \ 00000 \\ 0 \times 004 \ 00004 \\ 0 \times 004 \ 00008 \\ 0 \times 004 \ 0000 \ 0 \\ 0 \times 004 \ 00010 \\ 0 \times 004 \ 00014 \end{array}$ | or slt beq add addi j | \$2,\$0,\$0 \$8,\$0,\$5 \$8,\$0,3 \$2,\$2,\$4 \$5,\$5,-1 0x100001 | | |
| Next step: translate to more meaningful instructions (fix the branch/jump and add labels) Remember: jump address add 00 to end | | | | |

| Decoding Example (5/6) | | | | |
|--|-------------------------|---|----|--|
| ° MIPS Assembly (Part 2): | | | | |
| Loop : | or slt beq add | \$v0,\$0,\$0 \$t0,\$0,\$a1 \$t0,\$0,Fin \$v0,\$v0,\$a0 \$a1 \$a1 =1 | | |
| Fin: | j | Loop | | |
| ^o Next step: translate to C code (be creative!) | | | | |
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| Logical Operators (2/4) ° Truth Table: standard table listing all possible combinations of inputs and resultant output for each | | | | | |
|--|----------------|---------|---------|----------|----|
| °T | ruth 1 | Table | for ANI |) and OR | |
| | A | В | AND | OR | |
| | 0 | 0 | 0 | 0 | |
| | 0 | 1 | 0 | 1 | |
| | 1 | 0 | 0 | 1 | |
| | 1 | 1 | 1 | 1 | |
| | | | | | |
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| Logical Operators (3/4) |
|---|
| °Logical Instruction Syntax: |
| 1 2,3,4 |
| • where |
| 1) operation name |
| 2) register that will receive value |
| 3) first operand (register) |
| 4) second operand (register) or immediate (numerical constant) |
| |
| |
| |















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| Things to Remember (3/3) | | | |
|----------------------------------|--|--|--|
| ° New Instructions: | | | |
| and, andi, or, ori | | | |
| sll, srl, sra | | | |
| | | | |
| | | | |
| | | | |
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