DRAM Fab partnership for Intelligent RAM (IRAM)

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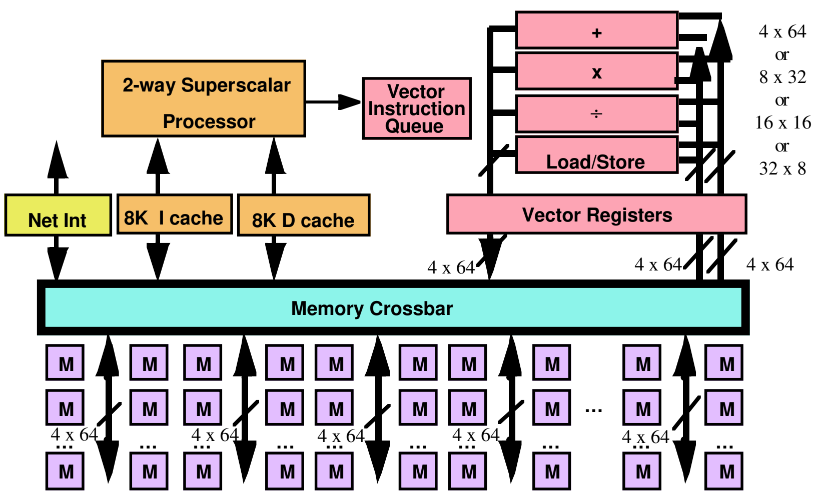
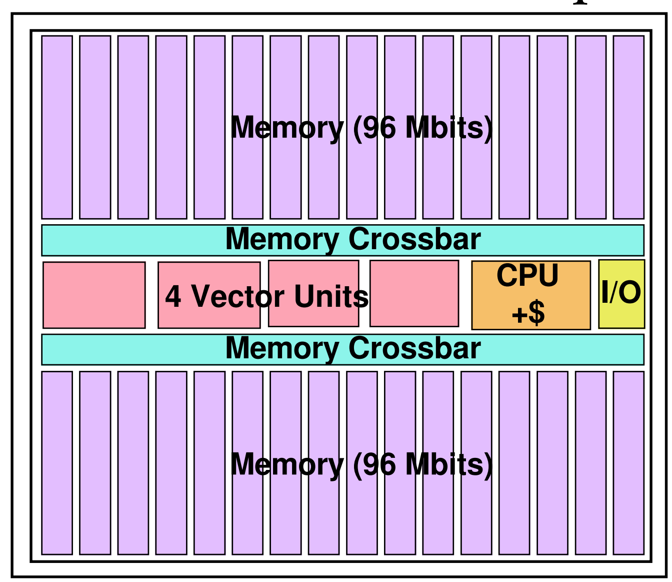
Outline

- Overview of V-IRAM-1
- Tentative Schedule
- Phases and Deliverables
- V-IRAM-1 SW/HW/Fab Tasks
- Requirements for Test Chips
- Requirements for V-IRAM-1 Prototype
- Where do we go from here?

V-IRAM-1: 0.25 µm, Fast Logic, 500 Mhz 4 GFLOPS(64b)/32 GOPS(8b)/24MB



V-IRAM-1 Floorplan



- 0.25 µm, 256 MbDRAM
- Die size = DRAM die
- 256M Xtors: 80% Memory, 8% Vector, 6% CPU ⇒ regular design

Goals for Vector IRAM Generations

- V-IRAM-1 (≈1999)
- 256 Mbit generation (0.25)
- Die size = 256 Mb DRAM die
- 1.5 - 2.0 v logic, 0.5-2.0 watts
- 300 - 500 MHz
- 4 64-bit pipes/lanes
- 4 GFLOPS(64b)/32GOPS(8b)
- 30 - 50 GB/sec Mem. BW
- 24 MB capacity + DRAM bus
- PCI bus/ FC-AL (serial SCSI)

- V-IRAM-2 (≈2002)
- 1 Gbit generation (0.18)
- Die size = 1 Gb DRAM die
- 1.0 - 1.5 v logic, 0.5-2.0 w
- 500 - 1000 MHz
- 8 64-bit pipes/lanes
- 16 GFLOPS/128GOPS
- 100 - 200 GB/sec Mem. BW
- 96 MB cap. + DRAM bus
- Many Gbit Ethernet/FC-AL

V-IRAM-1 Tentative Plan

- Phase I: Feasibility stage (≈H1'98)
  - Test chip, CAD agreement, architecture defined
- Phase 2: Design Stage (≈H2'98)
  - Simulated design
- Phase 3: Layout & Verification (≈H2'99)
  - Tape-out
- Phase 4: Fabrication,Testing, and Demonstration (≈H1'00)
  - Functional integrated circuit

Phase I: Feasibility Stage

- Berkeley Deliverables
  - White Paper, Architecture, Project Schedule
- Partner Deliverables
  - HSPICE, Design Rules, PAD Design, Cell Library?
  - Prototype runs for test chip (2 times?)
- Milestones
  - Test chip working, architecture defined, CAD agreement

(Test chip to exercise tools and partner relationship as well as DRAM/logic circuits)

Phase 2: Design Stage

- Berkeley Deliverables
  - HDL description of logic portion of IRAM, compilers, software libraries
- Partner Deliverables
  - DRAM Design, PAD design, Cell Library
  - Prototype runs for test chip in 256Mbit process?
- Milestones
  - Simulated design

Phase 3: Layout and Verification

- Berkeley Deliverables
  - Test vectors
- Partner Deliverables
  - DRAM layout, PAD layout
- Milestone
  - Tape-out

Phase 4: Fabrication,Testing, and Demonstration

- Berkeley Deliverables
  - Prototype PCB, Testing
- Partner Deliverables
  - Packaged parts, Test rig
- Milestone
  - Functional integrated circuit

V-IRAM-1 Software Tasks

- Libraries
  - Vector/Graphic/Image
  - BLAS
  - I/O Kernel
- OS
- Compilers
  - Scalar C compiler
  - Vector C compiler
- Instruction set level simulator

- Who does it?
  - Berkeley
  - Berkeley
  - Berkeley
- Berkeley
- Compilers
  - Partner?
  - Berkeley
- Berkeley

V-IRAM-1 Hardware Tasks

- Reg. Trans. Level simulator
  - Scalar Processor
  - Vector Unit/Memory System
- Circuits/Layout/Schematics
  - Processor
  - Caches
  - Vector Unit
    - » Fl. Point Unit/Datapath Generator?
  - Crossbar
  - DRAM Modules
  - Fast Serial I/O

- Who does it?
  - Partner?
  - Berkeley
-
  - Partner?
  - Partner?
  - Berkeley
    - » Partner?
  - Berkeley
  - Partner
  - Berkeley

V-IRAM-1 Validation/Fab Tasks

Simulation/Validation	Berkeley
Fabrication	Partner
Wafer test	Joint plan
– DRAM	– Partner
– Logic	– Berkeley?
Packaging	Partner?
Testing packaged parts	Berkeley?
Board design (copies for both)	Berkeley
Demo (copies for both)	Berkeley
ISSCC paper	Joint!

Phase I: Requirements for Test Chips

- CAD Design Flow
- General Design Information
- DRAM Macrocell description
- Testing plan/strategy
  - Work on together? (logic and DRAM)
- Someone to answer questions/visitor at UCB?
- Letter of understanding and wafer foundry agreement or prototype service agreement

Requirements for Test Chips

- CAD Design Flow
  - What is it at Partner's company?
  - What CAD tools should we buy?
  - What CAD tools should we borrow?
- One example set:
  - Layout: Cadence Dracula
  - Schematic Entry: Cadence ICDE (Integrated Circuit Design Environment)
  - Circuit: HSPICE
  - Logic Synthesis/Simulations: Synopsys
  - Cell Library: ??

Requirements for Test Chips

- General Design Information:
  1. HSPICE device model parameters (typical, fast, slow)
  2. Process Parameters: Cadence DRACULA LPE file
  3. Design rules file: Cadence DRACULA DRC file
  4. Electrical rules file: Cadence DRACULA ERC command file
  5. Cadence DRACULA LVS command file
  6. I/O pads layout

Requirements for Test Chips

- DRAM Macrocell
  1. Available configuration
     » Layout area, number of inputs/outputs, location of pins
  2. Power requirements
     » Routing requirement, peak and average current
  3. Interface timing
     » Access time, clock timing, signal level
  4. Guidelines of metal routing over array
  5. Refresh rate and cycles

Desired for V-IRAM-1 Prototype

- 0.25 micron, fast transistor, ≥4 metal layers
- "Fast" turnaround/testing
- Flexible interface to DRAM modules
- Scalar processor in that process?
- Group (not at UCB) to help with design?
- Testing plan/strategy
- Someone to answer questions/visitor at UCB?
- Letter of understanding and wafer foundry agreement or prototype service agreement

Specific Questions

- Scalar processor available for V-IRAM-1?
  – Clock rate, power, area, pipeline, floating point, superscalar, performance on benchmarks
- Technology for test chips, V-IRAM-1
  Logic: $L_{effective}$, V_t, V_{cc}; C_{cc} x V_{dd} / I_{sat}
  DRAM: cell size, V_t, V_{cc}
- Scaling logic across generations? (drop-in DRAM)
  – Simplified logic design rules span DRAM generations? e.g., Test chip 1 (Spring '98) in 4th Gen. 64Mb;
  Test chip 2 (Spr '99)/V-IRAM-1 (Fall '99) in 2G 256Mb

Specific Questions (cont'd)

- What is maturity of proposed technology?
  – Engineering samples, first customer ship, mass production?
  – How long is process available to fab in?
  – Technology roadmap for DRAM, merged logic?
- Test chip die size limits? Larger than DRAM die?
- V-IRAM=1 die size limit? Larger than DRAM die?
- Packaging options?
  – Ball grid array?

Where do we go from here?

- Partner determines if is interested or not
- Partner proposes what resources/technology can provide UCB, plan for prototype
- Pick 2 partners for test chips
- Depending on results/relationship/business plans, pick 1 partner for V-IRAM-1 prototype
- Even if not prototype partner, companies can participate in IRAM project, supporting students, attending two retreats per year, ...
- Other issues?