
Vector IRAM 1 Micro-architecture

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Outline

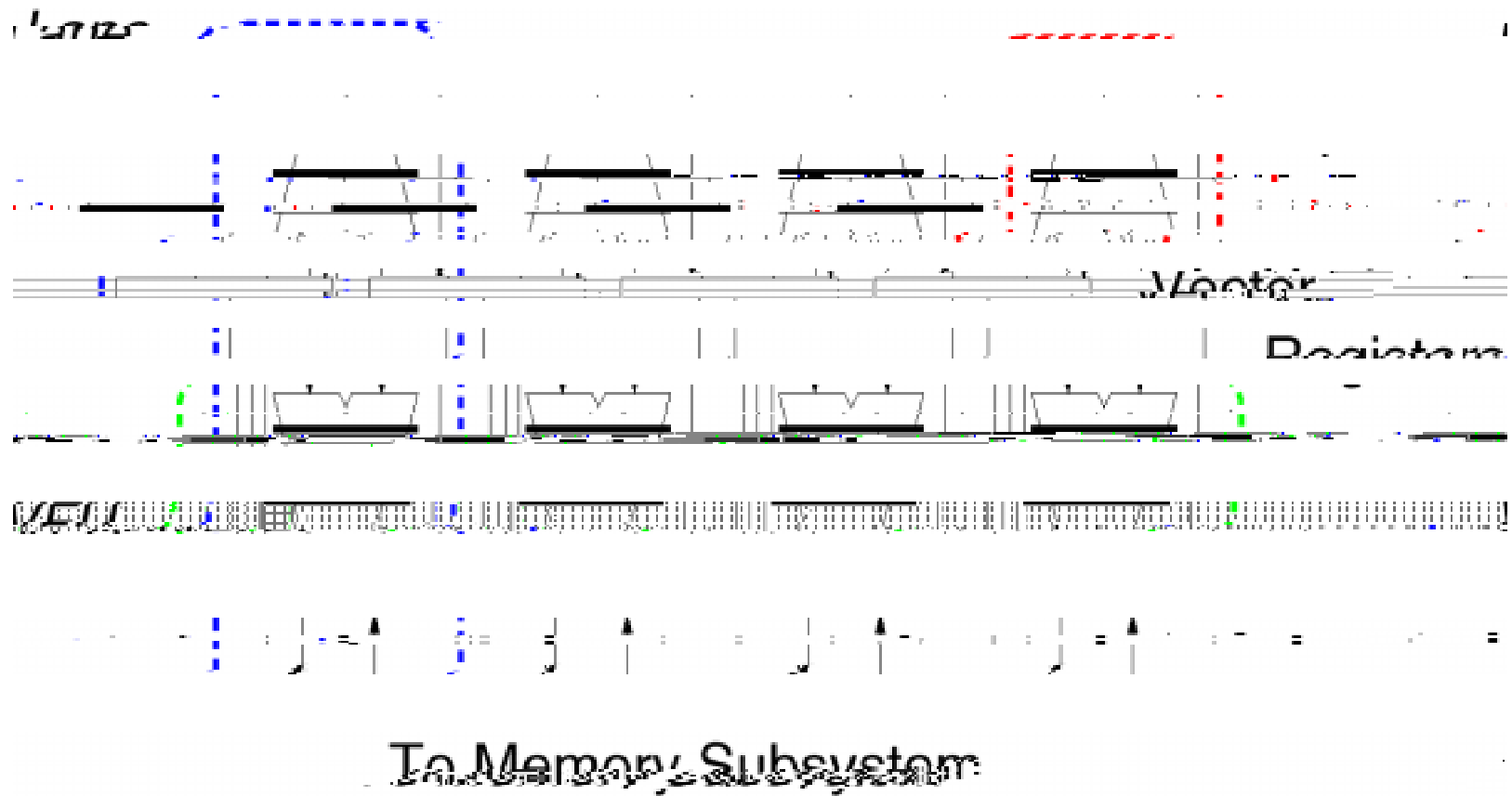
- Vector Unit
 - pipeline model
 - functional units
 - register file design
 - chaining
 - conditional execution support
 - performance monitoring
- Memory system
 - organization
 - data layout
 - TLB design
 - crossbar design
- I/O



VIRAM-1 Pipeline Model



Vector Lanes





Conditional Execution Support

- Vector length trimming

Performance Monitoring

- All counters 64-bit, accessed through vector control registers
- Cycle counter
- Target cycle 6 -1.202 " a//63.u generationnter• genera-3(11 c

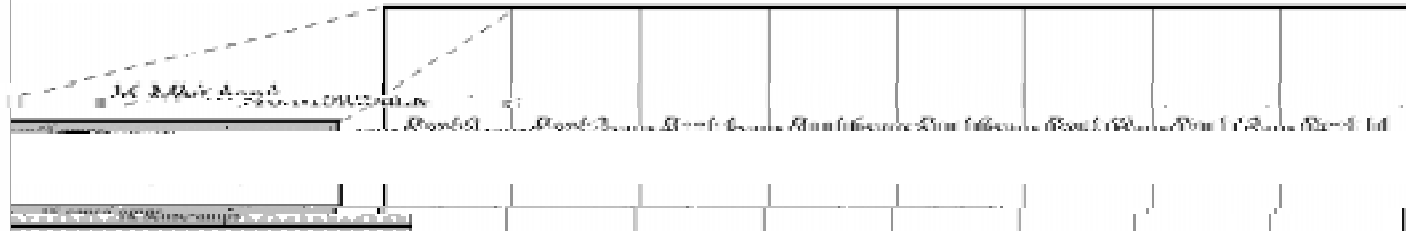
Performance Monitoring (cont.)

- Histogram RAM
 - hold a set of counters; can read/modify/write one per cycle

VIRAM-1 Memory System Overview

- 32 or 16 MB DRAM
- 2 memory wings
 - 8 banks per wing
 - 8 2Mbit sub-banks per bank

VI M-1 Floorplan



Data Layout in Memory

- Sub-bank row interleaving

10 3 3 1 5 3

- Examining the potential of: 256-bit super-word interleaving

10 3 3 3 1 2 3

- potential of less conflicts for strided/indexed accesses
- higher delay for cache refills; less energy efficient for unit stride
- if useful, we will support a per-process selection scheme between the two layouts

VIRAM-1 I/O

- 4 Gbit/sec serial I/O blocks