Lecture 36: Portable Computers—Processor Case Studies AT&T Hobbit, ARM, Lo Pwr Power PC

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“Embedded” Processor Families

- PowerPC
- Fujitsu, National introduce new architectures
- Intel, AMD: 386 processor cores
- ARM
- Motorola 68K processor cores
- Hitachi SH7000 series: Sega game machines
  - Best selling RISC processor!
- NEC V800 series

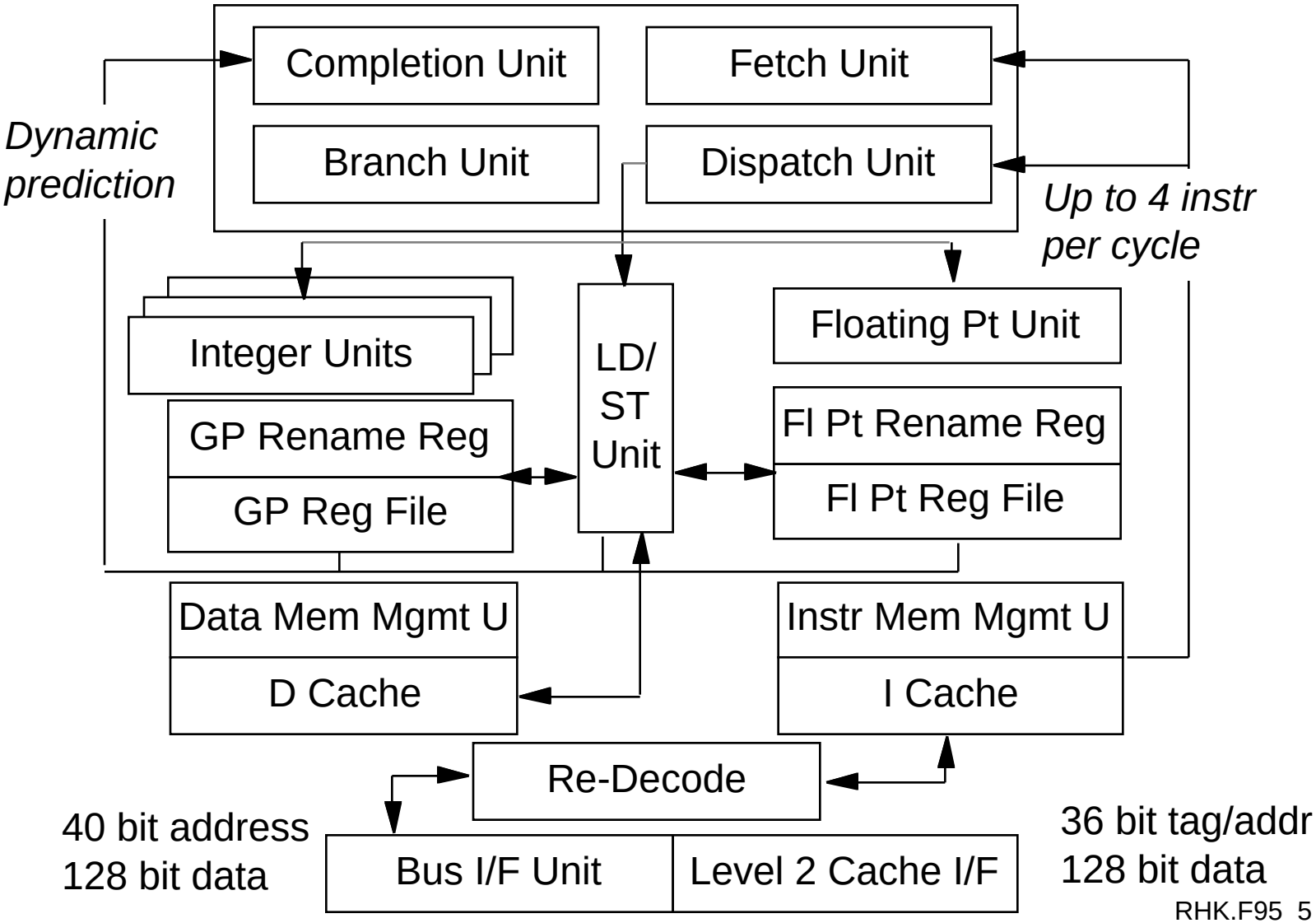
New Performance Metrics

- **MIPS/Watt**
  - **Battery life**
  - **Heat dissipation limits**
- **MIPS/sq. mm**
  - **Processor cores surrounded by specialized support functions**
  - **Reduced processor cost**
- **Bytes/task**
  - **Code density, where RAM/ROM space is at a premium**

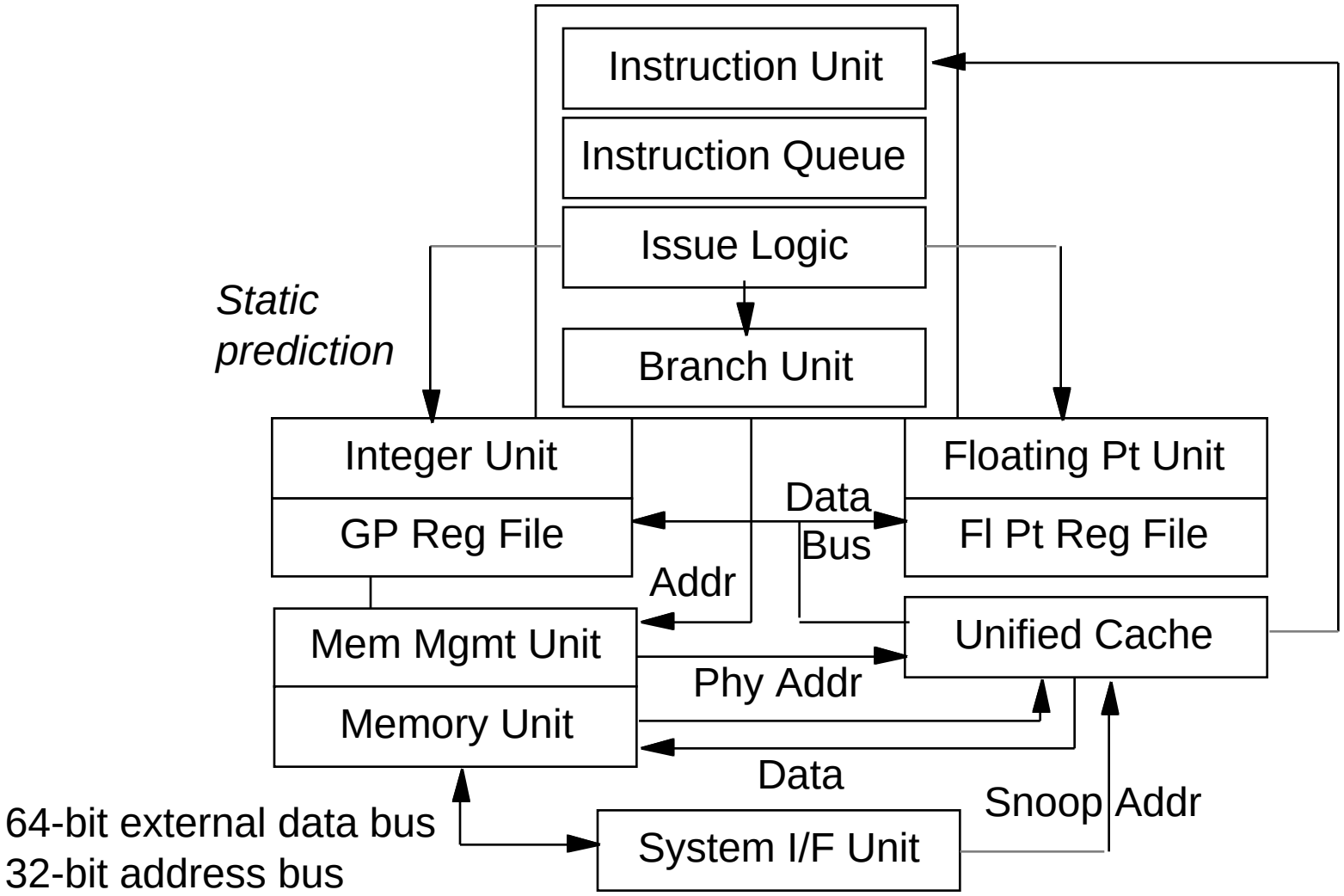
PowerPC

- **History**
  - **IBM Power Series (“Performance Optimized With Enhanced RISC”)**
  - **RS/6000 workstation (February 1990)**
  - **Joint development of IBM, Motorola, Apple**
  - **RS/6000 model 250 (September 1993), first use of PowerPC 601 chip**

PowerPC 620


Completion Unit
Fetch Unit
Branch Unit
Dispatch Unit
Dynamic prediction
Up to 4 instr per cycle
Integer Units
GP Rename Reg
GP Reg File
LD/ ST Unit
Floating Pt Unit
Fl Pt Rename Reg
Fl Pt Reg File
Data Mem Mgmt U
D Cache
Instr Mem Mgmt U
I Cache
Re-Decode
40 bit address
128 bit data
Bus I/F Unit
Level 2 Cache I/F
36 bit tag/addr
128 bit data

PowerPC 601


Instruction Unit
Instruction Queue
Issue Logic
Branch Unit
Static prediction
Integer Unit
GP Reg File
Floating Pt Unit
Fl Pt Reg File
Data Bus
Addr
Mem Mgmt Unit
Memory Unit
Unified Cache
Phy Addr
Data
Snoop Addr
64-bit external data bus
32-bit address bus
System I/F Unit

620 vs. 601

- **620**
  - **Dynamic branch prediction**
  - **Six execution units**
  - **Independent I and D caches on-chip**
  - **64-bit internal data paths**
  - **Support for off-chip Level 2 cache**
- **601**
  - **Static branch prediction**
  - **Three execution units**
  - **Unified I and D cache**
  - **32-bit internal data paths**

Other Members of the Family

- **602**
  - **Low power consumer multimedia applications**
  - **Ld/St unit added to 3 execution units of 601**
  - **System register for embedded processor support**
- **603**
  - **Portable applications, like PDAs and laptops**
  - **Dynamic power management**
- **604**
  - **like 620 but 32-bit internal design, no level 2 cache support**

PowerPC 602

- **Feature reduced version of 603**
  - **Smaller caches, TLB size**
  - **Elimination of superscalar dispatch**
  - **Simpler system bus (multiplexed/reduced pins)**
  - **SP FPU only**
  - **One half power, one third cost**
- **Some enhancements**
  - **Reduced cache store latency, support for unaligned cache access (good for graphics programs with many stores)**
  - **Reduced integer multiply latency**
- **1.0 million transistors, 50 sq mm, $14 manufacturing cost**

602 vs. 603

	602		603	
	Thruput	Latency	Thruput	Latency
Integer multiply, 8x32	1	2	2	2
Integer multiply, 16x32	2	3	3	3
Integer multiply, 32x32	4	5	5	5
Integer divide	37	37	37	37
FP add (SP)	1	3	1	3
FP multiply (SP)	1	3	1	3
FP multiply-add (SP)	1	3	1	3
FP divide (SP)	16	18	16	18

602 vs. 603

	602	603
CPU Clock Speed	66 Mhz	80 Mhz
Instr Fetch per Cycle	1	2
Instruction Queue	4	8
Instr Dispatch per Cycle	1+branch	2+branch
Completion Unit	4	5
Integer Unit	Fast multiply	Standard
FP Unit	Single precision	Single/Double
Load/Store Unit	Simplified	Standard
Hit under Miss	Yes	No
Store Latency	1 Cycle	2 Cycle
Instr/Data TLB size	32 / 32	64 / 64
Bus Type	mux	non-mux
Bus Width	64	32 or 64
Pwr Diss	1.2 W	2.5 W
Die Size	50 sq mm	85 sq mm
Manufacture Cost (est)	$14	$45
SPECint92 (est)	40 int	75 int

PowerPC Family Summary

Parameters	601	601v	602	603	603e	604	620
Architecture							
Reg Width, Bits	32	32	32	32	32	32	64
Addr Bus Width	32	32	32	32	32	32	40
Data Bus Width	64	64	64 (muxd)	32/64	32/64	64	128
Cache							
Data KB	32	32	4	8	16	16	32
Instr	(combined)	(combined)	4	8	16	16	32
Lvl 2?	Yes	Yes	No	No	No	No	Yes
Scalarity							
Instr/clock	3	3	3	3	3	4	4
Functional Units	3	3	4	5	5	6	6
CMOS Technology							
Op Voltage V	3.6	2.5	3.3	3.3	3.3	3.3	3.3
Design Rule µm	0.6	0.5	0.5	0.5	0.5	0.5	0.5
Die Size, mm sq	120	74	50	83	98	197	311
Mill transistors	2.8	2.8	1.0	1.6	2.6	3.6	7.0
Performance							
Op Freq (MHz)	80	100	66	66/80	100	100	133
SpecFP92	105	125		70/85	105	165	300
Specint92	85	105	40	60/75	120	160	225
Pwr Consump W	10	6	1.2	3(@80)	3.5	13	30

MIPS R4100

- 64-bit implementation from NEC
- 45 Dhrystones @ 40 MHz
- Multiply/Add instruction to support signal processing applications
  - Virtual modem, audio synthesis, video game acceleration
  - 40 million 16 x 16 + 64 -> 64-bit Mult/Add instr per second
- Exceptionally low power consumption
- Decended from MIPS 4200 architecture
  - 64-bit register set
  - All MIPS-III instructions
  - Conditional traps/branches/64-bit arithmetic
  - Identical MMU/TLB, 5-stage pipeline

MIPS R4100

- **Power Conservation Modes**
  - **Standby mode suspends internal operation, but cycles bus; 90% cut in power consumption**
  - **Suspend mode halts all activity; 95% cut in power**
  - **External interrupt wakes up processor in a few clock cycles**
  - **Hibernation mode shuts down whole processor; hard reset needed to resurrect**
- **Technology**
  - **0.5 µm 3-layer metal CMOS process**
- **Pricing**
  - **Sample: $50; 100,000 units: $25**

Dhrystone MIPS vs. Typ Pwr

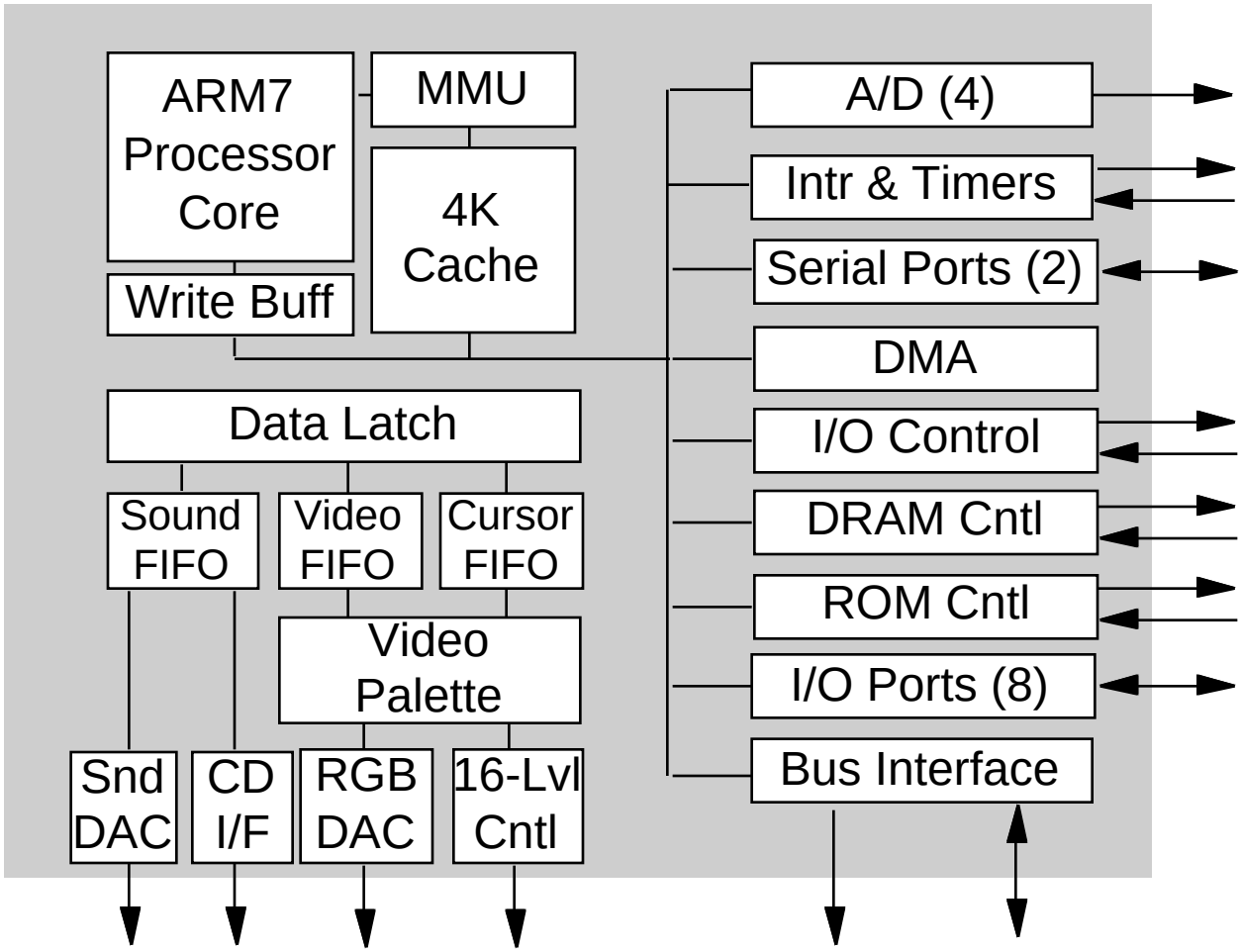
Processor	Speed	Power	MIPS/W
R4100@2.5V	25 MIPS	27 mW	929
R4100@3.3V	45 MIPS	120 mW	375
ARM710@3.3V	25 MIPS	100 mW	250
ARM710@5.0V	35 MIPS	450 mW	77
Intel 960JA@3.3V	30 MIPS	500 mW	60

Crucial figure of merit

ARM 7500

- **Integrated multimedia processor for set-top boxes**
  - **32-bit ARM core**
  - **MMU, 4K unified I and D cache**
  - **Audio/video functions integrated on-chip**
  - **33 MHz, 1.0 W (0.5 w/o RGB video DAC), 30 Dhrystone MIPS**
- **8-bit audio, 256-bit color video, 16 million color palette, 16-gray level support**
- **Direct support for RAS/CAS/WE signaling, automatic DRAM refresh logic**
- **PCMCIA support chip interface**

ARM 7500


ARM7
Processor
Core
MMU
4K
Cache
Write Buff
Data Latch
Sound
FIFO
Video
FIFO
Cursor
FIFO
Video
Palette
Snd
DAC
CD
I/F
RGB
DAC
16-Lvl
Cntl
A/D (4)
Intr & Timers
Serial Ports (2)
DMA
I/O Control
DRAM Cntl
ROM Cntl
I/O Ports (8)
Bus Interface