

Sanjit A. Seshia

Curriculum Vitae

Department of Electrical Engineering & Computer Sciences
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Research Interests

Dependable Computing, Computational Logic, Formal Methods, Electronic Design Automation, Embedded Systems, Computer Security, Program Analysis, Theory.

Academic Appointments

- 07/2011-date **University of California, Berkeley, USA**
Associate Professor
Department of Electrical Engineering and Computer Sciences
- 07/2005-06/2011 **University of California, Berkeley, USA**
Assistant Professor
Department of Electrical Engineering and Computer Sciences

Education

- 1998-2005 **Carnegie Mellon University, Pittsburgh, USA**
- ***Ph.D. in Computer Science*** (May 2005)
Thesis: Adaptive Eager Boolean Encoding for Arithmetic Reasoning in Verification
Advisor: Prof. Randal E. Bryant
Committee: Prof. Randal E. Bryant, Prof. Edmund M. Clarke, Prof. Jeannette M. Wing,
and Prof. David L. Dill
 - ***M.S. in Computer Science*** (August 2000)
- 1994-1998 **Indian Institute of Technology Bombay, India**
- ***B.Tech. in Computer Science & Engineering*** (May 1998)
GPA: 9.44/10
Thesis: Multisensor Image Alignment and Fusion
Advisors: Prof. Sharat Chandran and Prof. Rakesh Lal

Selected Awards and Honors

- Presidential Early Career Award for Scientists and Engineers – PECASE
Awarded by the White House in 2008; one of 67 awardees nation-wide in all fields of science and engineering
- Alfred P. Sloan Research Fellowship (2008)
- Hellman Family Faculty Fund Award, UC Berkeley (2008)
- NSF CAREER Award (2007)

- School of Computer Science Distinguished Dissertation Award, Carnegie Mellon University (2005)
Nominated for 2005 ACM Doctoral Dissertation Award
- National Defense Science and Engineering Graduate (NDSEG) Fellowship (1999-2002)
- Indian National Mathematics Olympiad Awardee (1993)
- National Talent Search (NTS) Scholarship, India (1992-1998)

Previous Work Experience

Carnegie Mellon University, Pittsburgh, PA, USA

Graduate Research Assistant

September 1998 – May 2005

Teaching Assistant

Fall 1999 & Fall 2001

Compaq/HP Systems Research Center, Palo Alto, CA, USA

Intern

May 2001 – August 2001

Consultant

September 2001 – May 2002

Cadence Berkeley Laboratories, Berkeley, CA, USA

Intern

May 1999 – August 1999

Indian Institute of Technology Bombay, Mumbai, India

Undergraduate Research Assistant

January 1997 – June 1998

Tata Institute of Fundamental Research, Mumbai, India

Intern, Visiting Student Research Program

May 1997 – July 1997

Publications

(Electronic copies of papers are available at <http://www.eecs.berkeley.edu/~sseshia/#pubs>.)

Book, Book Chapter, and Ph.D. Thesis

- *Introduction to Embedded Systems: A Cyber-Physical Systems Approach*,
Edward A. Lee and Sanjit A. Seshia,
First Edition, <http://LeeSeshia.org>, 2011.
- *Satisfiability Modulo Theories*,
Clark Barrett, Roberto Sebastiani, Sanjit A. Seshia, and Cesare Tinelli,
Chapter in Handbook of Satisfiability, IOS Press, 2009.
- *Adaptive Eager Boolean Encoding for Arithmetic Reasoning in Verification*,
Sanjit A. Seshia,
Ph.D. Thesis, Carnegie Mellon University, May 2005.
Co-winner, 2005 SCS Distinguished Dissertation Award.

Refereed Conference and Journal Papers

1. Sanjit A. Seshia and Alexander Rakhlin,
Quantitative Analysis of Systems Using Game-Theoretic Learning,
ACM Transactions on Embedded Computing Systems (ACM TECS), to appear.
2. John C. Eidson, Edward A. Lee, Slobodan Matic, Sanjit A. Seshia, and Jia Zou,
Distributed Real-Time Software for Cyber-Physical Systems, Proceedings of the IEEE, to appear.

3. Jonathan Kotker, Dorsa Sadigh, and Sanjit A. Seshia,
Timing Analysis of Interrupt-Driven Programs under Context Bounds,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), October 2011, to appear.
4. Bryan Brady, Randal E. Bryant, and Sanjit A. Seshia,
Learning Conditional Abstractions,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), October 2011, to appear.
5. Susmit Jha, Sanjit A. Seshia, and Ashish Tiwari,
Synthesis of Optimal Switching Logic for Hybrid Systems,
In Proceedings of the 11th International Conference on Embedded Software (EMSOFT), October 2011, to appear.
6. Wenchao Li, Lili Dworkin, and Sanjit A. Seshia,
Mining Assumptions for Synthesis,
In Proceedings of the 9th ACM/IEEE International Conference on Formal Methods and Models for Code-sign (MEMOCODE), July 2011, to appear.
7. Daniel Holcomb, Bryan Brady, and Sanjit A. Seshia,
Abstraction-Based Performance Analysis of NoCs,
In Proceedings of the Design Automation Conference (DAC), pages 492–497, June 2011.
8. Sanjit A. Seshia and Jonathan Kotker,
GameTime: A Toolkit for Timing Analysis of Software,
Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), pages 388–392, March 2011.
9. Bryan Brady, Daniel Holcomb, and Sanjit A. Seshia,
Counterexample-Guided SMT-Driven Optimal Buffer Sizing,
Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 329–334, March 2011.
10. Pierluigi Nuzzo, Alberto Puggelli, Sanjit A. Seshia, and Alberto Sangiovanni-Vincentelli,
CalCS: SMT Solving for Non-Linear Convex Constraints,
In Proceedings of the IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD), pages 71–79, October 2010.
11. Bryan Brady, Randal E. Bryant, Sanjit A. Seshia, and John W. O’Leary,
ATLAS: Automatic Term-Level Abstraction of RTL Designs,
In Proceedings of the Eighth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), pages 31–40, July 2010.
12. Wenchao Li, Alessandro Forin, and Sanjit A. Seshia,
Scalable Specification Mining for Verification and Diagnosis,
In Proceedings of the Design Automation Conference (DAC), pages 755–760, June 2010.
13. Susmit Jha, Sumit Gulwani, Sanjit A. Seshia and Ashish Tiwari,
Oracle-Guided Component-Based Program Synthesis,
In Proceedings of the International Conference on Software Engineering (ICSE), pages 215–224, May 2010.
14. Susmit Jha, Sumit Gulwani, Sanjit A. Seshia and Ashish Tiwari,
Synthesizing Switching Logic for Safety and Dwell-Time Requirements,
In Proceedings of the International Conference on Cyber-Physical Systems (ICCPS), pages 22–31, April

- 2010.
15. Dave King, Susmit Jha, Divya Muthukumar, Trent Jaeger, Somesh Jha, and Sanjit A. Seshia, *Automating Security Mediation Placement*, In Proceedings of the European Symposium on Programming (ESOP), pages 327–344, March 2010.
 16. Cynthia Sturton, Susmit Jha, Sanjit A. Seshia, and David Wagner, *On Voting Machine Design for Verification and Testability*, Proceedings of the 16th ACM Conference on Computer and Communications Security (CCS), pages 463–476, November 2009.
 17. Susmit Jha, Rhishikesh Limaye, and Sanjit A. Seshia, *Beaver: Engineering an Efficient SMT Solver for Bit-vector Arithmetic*, Proceedings of the 21st International Conference on Computer-Aided Verification (CAV), pages 668–674, June 2009.
 18. Daniel E. Holcomb, Wenchao Li, and Sanjit A. Seshia, *Design as You See FIT: System-Level Soft Error Analysis of Sequential Circuits*, Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 785–790, April 2009.
 19. Wenchao Li, Marco Di Natale, Paolo Giusto, Wei Zheng, Alberto Sangiovanni-Vincentelli, and Sanjit A. Seshia, *Optimizations of an Application-Level Protocol for Enhanced Dependability in FlexRay*, Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 1076–1081, April 2009.
 20. Randal E. Bryant, Daniel Kroening, Joël Ouaknine, Sanjit A. Seshia, Ofer Strichman, and Bryan Brady, *An Abstraction-Based Decision Procedure for Bit-Vector Arithmetic*, In International Journal on Software Tools for Technology Transfer (STTT), vol. 11(2), pages 95–104, 2009.
Earlier version appeared as *Deciding Bit-Vector Arithmetic with Abstraction*, Proceedings of the International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), LNCS 4424, pages 358–372, March 2007.
 21. Sanjit A. Seshia and Alexander Rakhlin, *Game-Theoretic Timing Analysis*, In Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pages 575–582, November 2008.
 22. Orna Kupferman, Wenchao Li, and Sanjit A. Seshia, *A Theory of Mutations with Applications to Vacuity, Coverage, and Fault Tolerance*, In Proceedings of the IEEE International Conference on Formal Methods in Computer-Aided Design (FMCAD), November 2008.
 23. Dave King, Trent Jaeger, Somesh Jha, and Sanjit A. Seshia, *Effective Blame for Information-Flow Violations*, In Proceedings of the 16th ACM SIGSOFT International Symposium on Foundations of Software Engineering (FSE), pages 250–260, November 2008.
 24. Susmit K. Jha, Bryan Brady, and Sanjit A. Seshia, *Symbolic Reachability Analysis of Lazy Linear Hybrid Automata*, In Proceedings of the International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS), pages 241–256, October 2007.

25. Sanjit A. Seshia, K. Subramani, and Randal E. Bryant,
On Solving Boolean Combinations of UTVPI Constraints,
Journal of Satisfiability, Boolean Modeling, and Computation (JSAT), vol. 3, pages 67–90, 2007.
26. Dirk Beyer, Arindam Chakrabarti, Thomas A. Henzinger, and Sanjit A. Seshia,
An Application of Web-Service Interfaces,
In Proceedings of the IEEE International Conference on Web Services (ICWS), pages 831–838, July 2007.
27. Sanjit A. Seshia,
Autonomic Reactive Systems via Online Learning,
Proceedings of the IEEE International Conference on Autonomic Computing (ICAC), June 2007.
28. Armando Solar-Lezama, Gilad Arnold, Liviu Tancau, Rastislav Bodik, Vijay Saraswat, and Sanjit A. Seshia,
Sketching Stencils,
ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), pages 167–178, June 2007.
29. Sanjit A. Seshia, Wenchao Li, and Subhasish Mitra,
Verification-Guided Soft Error Resilience,
Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 1442-1447, April 2007.
30. Huining T. Feng, Lynn T-N. Wang, Wei Zheng, Sri Kanajan, and Sanjit A. Seshia,
Automatic Model Generation for Black Box Real-Time Systems,
Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 930-935, April 2007.
31. Armando Solar-Lezama, Liviu Tancau, David Turner, Rastislav Bodik, Vijay Saraswat, and Sanjit A. Seshia,
Combinatorial Sketching for Finite Programs,
12th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), pages 404-415, ACM Press, October 2006.
32. Sanjit A. Seshia and Randal E. Bryant,
Deciding Quantifier-Free Presburger Formulas Using Parameterized Solution Bounds,
Logical Methods in Computer Science journal, vol. 1 (2:5), pages 1–26, December 2005.
Earlier version in 19th IEEE Symposium on Logic in Computer Science (LICS), pages 100–109, July 2004.
Among 10 invited papers from 40 accepted conference papers and 168 submissions.
33. Cormac Flanagan, Stephen N. Freund, Shaz Qadeer, and Sanjit A. Seshia,
Modular Verification of Multithreaded Programs,
Theoretical Computer Science, vol. 338, issues 1-3, 10 June 2005, pages 153–183.
Awarded “Top Cited Article, 2005-10” in this journal.
Earlier version in 14th International Conference on Computer-Aided Verification (CAV), LNCS 2404, pages 180–194, July 2002.
34. Mihai Christodorescu, Somesh Jha, Sanjit A. Seshia, Dawn Song, and Randal E. Bryant,
Semantics-Aware Malware Detection,
IEEE Symposium on Security and Privacy, Oakland, May 2005, pages 32–46.
35. Vinod Ganapathy, Sanjit A. Seshia, Somesh Jha, Thomas W. Reps, and Randal E. Bryant,
Automatic Discovery of API-Level Exploits,
27th International Conference on Software Engineering (ICSE), May 2005, pages 312–321.

36. Sanjit A. Seshia, Randal E. Bryant and Kenneth S. Stevens,
Modeling and Verifying Circuits Using Generalized Relative Timing,
11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), March 2005, pages 98–108.
Runner-up for best paper award.
37. Daniel Kroening, Joël Ouaknine, Sanjit A. Seshia, and Ofer Strichman,
Abstraction-Based Satisfiability Solving of Presburger Arithmetic,
16th International Conference on Computer-Aided Verification (CAV), LNCS 3114, pages 308–320, July 2004.
38. Shuvendu K. Lahiri and Sanjit A. Seshia,
The UCLID Decision Procedure (system description),
16th International Conference on Computer-Aided Verification (CAV), LNCS 3114, pages 475–478, July 2004.
39. Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia,
Convergence Testing in Term-Level Bounded Model Checking,
12th Conference on Correct Hardware Design and Verification Methods (CHARME), LNCS 2860, pages 348–362, October 2003.
40. Sanjit A. Seshia and Randal E. Bryant,
Unbounded, Fully Symbolic Model Checking of Timed Automata Using Boolean Methods,
15th International Conference on Computer-Aided Verification (CAV), LNCS 2725, pages 154–166, July 2003.
41. Sanjit A. Seshia, Shuvendu K. Lahiri, and Randal E. Bryant,
A Hybrid SAT-Based Decision Procedure for Separation Logic with Uninterpreted Functions,
40th Design Automation Conference (DAC), pages 425–430, June 2003.
Best paper finalist. In top 14 out of 152 accepted papers and 628 submissions.
42. Shuvendu K. Lahiri, Sanjit A. Seshia, and Randal E. Bryant,
Modeling and Verification of Out-of-Order Microprocessors Using UCLID,
4th International Conference on Formal Methods in Computer-Aided Design (FMCAD), LNCS 2517, pages 142–159, November 2002.
43. Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia,
Modeling and Verifying Systems Using a Logic of Counter Arithmetic with Lambda Expressions and Uninterpreted Functions,
14th International Conference on Computer-Aided Verification (CAV), LNCS 2404, pages 78–92, July 2002.
44. Ofer Strichman, Sanjit A. Seshia, and Randal E. Bryant,
Deciding Separation Formulas with SAT,
14th International Conference on Computer-Aided Verification (CAV), LNCS 2404, pages 209–222, July 2002.
45. Sanjit A. Seshia, R. K. Shyamasundar, Anup K. Bhattacharjee, and S. D. Dhodapkar,
A Translation of Statecharts to Esterel,
1st World Congress on Formal Methods (FM), LNCS 1709, pages 983–1007, September 1999.
46. Anup K. Bhattacharjee, S. D. Dhodapkar, Sanjit A. Seshia, and R. K. Shyamasundar,
PERTS: A Graphical Environment for the Specification and Verification of Reactive Systems,
Journal of Reliability Engineering and System Safety, 71(3), 2001, pages 299–310 (erratum: vol. 72(2)).
Earlier version in SAFECOMP’99, LNCS 1698, pages 431–444, September 1999.

Invited Papers and Tutorials

47. Jeff C. Jensen, Edward A. Lee, and Sanjit A. Seshia,
An Introductory Capstone Design Course on Embedded Systems,
In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2011.
48. Sanjit A. Seshia,
Quantitative Analysis of Software: Challenges and Recent Advances,
Invited paper at the 7th International Workshop on Formal Aspects of Component Software, October 2010.
49. Subhasish Mitra, Sanjit A. Seshia, and Nicola Nicolici,
Post-Silicon Validation: Opportunities, Challenges and Recent Advances,
Invited special session paper at the Design Automation Conference (DAC), pages 12–17, June 2010.
50. Edward A. Lee, Slobodan Matic, Sanjit A. Seshia, and Jia Zou,
The Case for Timing-Centric Distributed Software,
Invited paper at the 2nd International Workshop on Cyber-Physical Systems (WCPS), pages 57–64, June 2009.
51. Daniel Kroening and Sanjit A. Seshia,
Formal Verification at Higher Levels of Abstraction,
Invited tutorial at International Conference on Computer-Aided Design (ICCAD), pages 572–578, November 2007.
52. Randal E. Bryant and Sanjit A. Seshia,
Decision Procedures Customized for Formal Verification,
Invited paper at the Conference on Automated Deduction (CADE), pages 255–259, July 2005.

Refereed Workshop Papers

53. Edward A. Lee and Sanjit A. Seshia,
An Introductory Textbook on Cyber-Physical Systems,
In Workshop on Embedded Systems Education (WESE), ESWeek, October 2010.
54. Susmit Jha, Wenchao Li, and Sanjit A. Seshia,
Localizing Transient Faults Using Dynamic Bayesian Networks,
In IEEE International High Level Design Validation and Test (HLDVT) Workshop, November 2009.
55. Randal E. Bryant, Shuvendu K. Lahiri, and Sanjit A. Seshia,
Deciding CLU Logic Formulas via Boolean and Pseudo-Boolean Encodings,
1st International Workshop on Constraints in Formal Verification (CFV), associated with Principles and Practice of Constraint Programming (CP), September 2002.
56. Nicholas J. Hopper, Sanjit A. Seshia, and Jeannette M. Wing,
A Comparison and Combination of Theory Generation and Model Checking for Security Protocol Analysis,
Workshop on Formal Methods in Computer Security (FMCS), associated with Computer-Aided Verification (CAV), July 2000.

Technical Reports (those that do not overlap with the above papers)

57. Sanjit A. Seshia,
Sciduction: Combining Induction, Deduction, and Structure for Verification and Synthesis,
Technical report UCB/EECS-2011-68, EECS Department, UC Berkeley, May 2011.
58. Daniel Holcomb, Wenchao Li, and Sanjit A. Seshia,
Algorithms for Green Buildings: Learning-Based Techniques for Energy Prediction and Fault Diagnosis,
Technical report UCB/EECS-2009-138, EECS Department, UC Berkeley, October 2009.

59. John C. Eidson, Edward A. Lee, Slobodan Matic, Sanjit A. Seshia, and Jia Zou,
Time-centric Models For Designing Embedded Cyber-physical Systems,
Technical report UCB/EECS-2009-135, EECS Department, UC Berkeley, October 2009.
60. Sumit Gulwani and Sanjit A. Seshia, Eds.,
Proceedings of the 1st Workshop on Quantitative Analysis of Software (QA'09), Technical report UCB/EECS-2009-93, EECS Department, UC Berkeley, June 2009.
61. Susmit Jha, Sanjit A. Seshia, and Rishikesh Limaye,
On the Computational Complexity of Satisfiability Solving for String Theories,
Technical report UCB/EECS-2009-41, EECS Department, UC Berkeley, March 2009.
62. Bryan Brady, Randal E. Bryant and Sanjit A. Seshia,
Abstracting RTL Designs to the Term Level,
Technical report UCB/EECS-2008-136, EECS Department, UC Berkeley, October 2008.
63. Orna Kupferman, Wenchao Li, and Sanjit A. Seshia,
On the Duality between Vacuity and Coverage,
Technical report UCB/EECS-2008-26, EECS Department, UC Berkeley, March 2008.
64. Dave King, Susmit Jha, Trent Jaeger, Somesh Jha, and Sanjit A. Seshia,
On Automatic Placement of Declassifiers for Information-Flow Security,
Technical Report NAS-TR-0083-2007, Network and Security Research Center, Pennsylvania State University, November 2007.
65. Sanjit A. Seshia,
Integrated Verification for Robust Computing,
Technical report UCB/EECS-2006-103, EECS Department, UC Berkeley, July 2006.
66. Sanjit A. Seshia, Guy E. Blelloch, and Robert W. Harper,
A Performance Comparison of Interval Arithmetic and Error Analysis in Geometric Predicates,
CMU-CS-00-172, Computer Science Department, Carnegie Mellon University, December 2000.
67. Sanjit A. Seshia and Randal E. Bryant,
The Hardness of Approximating Minima in OBDDs, FBDDs and Boolean functions,
CMU-CS-00-156, Computer Science Department, Carnegie Mellon University, August 2000.

Talks

Invited Talks/Panels

1. *UCLID's Elements: Term-Level Verification and SMT Solving*,
Invited talk, SMT/SAT Summer School, MIT, Cambridge, MA, June 15, 2011.
2. *Verifying Timing-Centric Software Systems*,
Invited talk, 11th Annual Conference on High Confidence Software and Systems (HCSS), May 4, 2011.
3. *Voting Machines and Automotive Software: Explorations with SMT at Scale*,
Seminar on Deduction at Scale, Ringberg Castle, Germany, March 7, 2011.
4. *Quantitative Verification of Software: Challenges and Recent Advances*,
Invited talk, 24th IEEE International Conference on VLSI Design and 10th Conference on Embedded Software, Chennai, India, January 6, 2011.
Also given at Coverity, Inc., February 8, 2011.
5. *On Voting Machine Design for Verification and Testability*,
Invited talk, 2nd IEEE International Workshop on Reliability Aware System Design and Test, Chennai, India, January 6, 2011.

6. *The Challenge of Environment Modeling in Verifying Cyber-Physical Software Systems*,
Workshop on Usable Verification, Redmond, WA, November 15, 2010.
7. *Formal Methods for Dependable Computing: From Models, through Software, to Circuits*,
Invited talk, CITRIS Research Exchange, Berkeley, CA, November 3, 2010.
8. Invited panelist, *The Verification Challenge of Low-Level Embedded Software*,
IEEE International Conference on Formal Methods in Computer Aided Design (FMCAD), Lugano, Switzerland, October 22, 2010.
9. *Quantitative Analysis of Software: Challenges and Recent Advances*,
Keynote talk, 7th International Workshop on Formal Aspects of Component Software, Guimaraes, Portugal, October 16, 2010.
10. *Quantitative Verification and Synthesis of Systems*,
Invited talk, Strategic Directions in Software at Scale (SaS), Berkeley, CA, August 18, 2010.
11. *Integrating Induction and Deduction for Verification and Synthesis*,
Software Seminar, Computer Science Department, Stanford University, June 1, 2010.
12. *Voting Machine Design for Verification and Testability*,
Microsoft Research, Redmond, WA, March 19, 2010.
13. *Verification-Guided Error Resilience*,
Sundaram Seshu Scholar Lecture, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, October 29, 2008.
 - Also given at the CANDE Workshop, Pacifica, CA, November 8, 2008.
14. *Mutations for Evaluating Coverage and Fault Tolerance*,
Microsoft Research, Bangalore, India, August 5, 2008.
15. *Formal Verification at Higher Levels of Abstraction*,
Tutorial at International Conference on Computer-Aided Design (ICCAD), November 8, 2007.
16. *Diagnosis, Repair, and Multi-Armed Bandits*,
SRI International, Menlo Park, May 23, 2007.
17. *Adaptive Eager Boolean Encoding for Arithmetic Reasoning in Verification*,
SCS Distinguished Lecture Series, Carnegie Mellon University, February 2, 2006.
18. *SAT-Based Decision Procedures and Malware Detection*,
Software Seminar, Computer Science Department, Stanford University, November 29, 2005.
19. *Reasoning about Reliability and Security Using Boolean Methods*,
General Motors India Science Laboratory, July 21, 2005.
20. *UCLID: Deciding Combinations of Theories via Eager Translation to SAT*,
Stanford/SRI Summer School on Combination of Decision Procedures, August 10, 2004.
21. *The Small Model Property of Integer Linear Arithmetic*,
Computer Science and Artificial Intelligence Laboratory, Massachusetts Institute of Technology, July 22, 2004.
22. *First-Order Decision Procedures Based on Eager SAT-Encodings*,
Tata Institute of Fundamental Research, Mumbai, India, January 2, 2004.
23. *Translating Quantified Separation Logic to Quantified Boolean Logic*,
Dagstuhl Seminar on Deduction and Infinite-State Model Checking, Germany, April 24, 2003.
24. *A SAT-Based Decision Procedure for Infinite-State System Verification*,
Microsoft Research, Redmond, November 8, 2002.

25. *A Translation of Statecharts to Esterel*,
Microsoft Research, Cambridge, U.K., September 24, 1999.

Selected Conference Presentations

26. *Satisfiability Modulo Theories*,
Tutorial at International Conference on Computer-Aided Design (ICCAD), November 2, 2009.
27. *Game-Theoretic Timing Analysis*,
IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Jose, November 11, 2008.
28. *Teaching Embedded Systems to Berkeley Undergraduates*,
NSF Workshop “From Embedded Systems to Cyber-Physical Systems: A Review of the State-of-the-Art and Research Needs”, St. Louis, April 21, 2008.
29. *Autonomic Reactive Systems via Online Learning*,
4th International Conference on Autonomic Computing (ICAC), June 14, 2007.
30. *Verification-Guided Soft Error Resilience*,
10th International Conference on Design Automation and Test in Europe (DATE), April 19, 2007.
31. *Modeling and Verifying Circuits Using Generalized Relative Timing*,
11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), March 15, 2005.
32. *Deciding Quantifier-Free Presburger Arithmetic Using Parameterized Solution Bounds*,
19th Annual IEEE Symposium on Logic in Computer Science (LICS), July 14, 2004.
33. *Unbounded, Fully Symbolic Model Checking of Timed Automata Using Boolean Methods*,
15th International Conference on Computer-Aided Verification (CAV), July 10, 2003.
34. *A Hybrid SAT-Based Decision Procedure for Separation Logic with Uninterpreted Functions*,
40th Design Automation Conference (DAC), June 4, 2003.
35. *Modeling and Verifying Systems Using CLU Logic*,
14th International Conference on Computer-Aided Verification (CAV), July 28, 2002.
36. *A Translation of Statecharts to Esterel*,
1st World Congress on Formal Methods (FM), September 21, 1999.

Selected Seminars and Colloquia

37. *From Security to Cyber-Physical Systems: The Sciductive Approach to Verification and Synthesis*,
Joint CSE/EE Seminar, Indian Institute of Technology, Bombay, January 3, 2011.
38. *On Voting Machine Design for Verification and Testability*,
Tata Institute of Fundamental Research, Mumbai, December 28, 2010.
39. *Integrating Induction and Deduction for Verification and Synthesis*,
Given at the following venues:
 - University of Texas, Austin, TX, April 15, 2010.
 - PRECISE Center Seminar, University of Pennsylvania, Philadelphia, PA, May 19, 2010.
 - CMACS Seminar, Carnegie Mellon University, Pittsburgh, PA, May 21, 2010.
40. *Game-Theoretic Quantitative Analysis of Embedded Software*,
Given at the following venues:
 - Princeton University, Princeton, NJ, November 12, 2009.
 - EPFL, Lausanne, Switzerland, July 3, 2009.
 - Technical University of Vienna, Austria, July 10, 2009.
 - University of Salzburg, Austria, July 13, 2009.
 - Bruno Kessler Foundation (FBK), Trento, Italy, July 14, 2009.

41. *Game-Theoretic Timing Analysis*,
Given at the following venues:
 - CHES Seminar Series, UC Berkeley, September 23, 2008.
 - Microsoft Research, Redmond, WA, November 18, 2008.
 - Intel Strategic CAD Labs, Hillsboro, OR, November 21, 2008.
42. *Diagnosis, Repair, and Multi-Armed Bandits*,
DES/CHES Seminar, University of California, Berkeley, May 8, 2007.
43. *SAT-Based Decision Procedures and Software Security*,
Programming Systems Seminar, University of California, Berkeley, October 24, 2005.
44. *Reasoning about Timed Systems Using Boolean Methods*,
CHES Seminar, University of California, Berkeley, October 11, 2005.
45. *Boolean Methods in Computer Reliability and Security*,
Joint CSE/EE Seminar, Indian Institute of Technology, Bombay, August 11, 2005.
46. *Reasoning about Reliability and Security Using Boolean Methods*,
Given at the following venues:
 - Dept. of Computer Science and Engineering, UC San Diego, April 27, 2005.
 - Computer Sciences Department, University of Wisconsin, Madison, April 25, 2005.
 - Information Science and Technology Seminar, California Inst. of Technology, April 20, 2005.
 - Microsoft Research, Redmond, April 18, 2005.
 - EECS Special Seminar, Massachusetts Institute of Technology, April 14, 2005.
 - EECS Colloquium, University of California, Berkeley, April 6, 2005.
 - CSE Colloquium, University of Washington, Seattle, March 31, 2005.
 - Dept. of Electrical and Computer Engineering, University of Texas, Austin, March 24, 2005.
47. *Boolean Methods for Arithmetic Reasoning*,
Dept. of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, March 8, 2005.
48. *Modular Verification of Multithreaded Software*,
SCS Student Seminar Series, Carnegie Mellon University, April 12, 2002.

Teaching and Advising Experience

Teaching at UC Berkeley

- | | |
|------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Spring 2011,
Spring 2009 &
Spring 2008 | <i>Introduction to Embedded Systems</i> (EECS 149). Upper-division undergraduate course on embedded systems. This is a newly created undergraduate course at UC Berkeley, taught for the first time in Spring 2008. <ul style="list-style-type: none"> • The Spring 2008 offering was numbered EECS 124. Co-taught with Prof. Edward Lee in Spring 2011 and 2008. |
| Spring 2011,
Fall 2009,
Spring 2007 &
Spring 2006 | <i>Computer-Aided Verification</i> (EECS 219C). Advanced graduate course on formal verification with a focus on algorithmic techniques such as model checking and satisfiability solving (SAT/SMT). |

Fall 2010	<i>Fundamental Algorithms for System Modeling, Analysis, and Optimization</i> (EECS 144/244). A joint offering of an upper-division undergraduate course (144) and core graduate course (244) on fundamental algorithmic techniques underlying the design methodology for complex systems, using integrated circuit design as an example (co-taught with Prof. Edward Lee and Prof. Jaijeet Roychowdhury). EECS 144 is a newly created undergraduate course at UC Berkeley, taught for the first time in Fall 2010. The existing graduate course EECS 244 has been revised significantly.
Spring 2010, Spring 2008, & Fall 2006	<i>Computability and Complexity</i> (CS 172). Upper-division undergraduate course on automata theory, computability, and complexity theory.
Fall 2005, 2007, & 2008	<i>Introduction to Computer-Aided Design of Integrated Circuits</i> (EECS 244, co-taught with Prof. Kurt Keutzer). Core graduate course on CAD for ICs.
Fall 2007	<i>Current Berkeley Research in Programming Systems</i> (CS 294-25). Research-oriented graduate course in programming systems (co-taught with Professors R. Bodik, K. Sen, D. Song, and K. Yelick).

Past Teaching: As a graduate and undergraduate student, I served as a teaching assistant for classes on Computer Systems (CMU, 15-213), Algorithms (CMU, 15-451), and Introductory Programming (IIT Bombay, CS101).

Graduate Student Advisees

Current:

- Susmit Jha, Ph.D. in EECS (January 2007 – date)
- Wenchao Li, Ph.D. in EECS (August 2007 – date)
- Daniel Holcomb, Ph.D. in EECS (October 2008 – date)
- Jonathan Kotker, M.S. in EECS (August 2010 – date)

Graduated:

- Bryan Brady, Ph.D. in EECS (graduated May 2011)
- Rhishikesh Limaye, M.S. in EECS (graduated May 2010)

Undergraduate Advisees

- Dorsa Sadigh, Senior, EECS, UC Berkeley (January 2011 - date)
- Lisa Yan, Sophomore, EECS, UC Berkeley (January - May 2011)
- Johnny Lam, Junior, EECS, UC Berkeley (May - December 2010)
- Rohan Desai, Senior, EECS, UC Berkeley (May - June 2010)
- Lili Dworkin, Junior, Haverford College, SUPERB (NSF REU) participant (June - August 2010)
- Min Xu, Senior, EECS, UC Berkeley (August 2008 - June 2009)
- Jeff Jensen, Senior, EECS, UC Berkeley (August - December 2008)
- Lei Huang, Senior, EECS, UC Berkeley (August - December 2008)
- Adam Harwayne, Senior, EECS, UC Berkeley (August - December 2008)
- Daniel Wong, Senior, EECS, UC Berkeley (January - June 2008)

- Kedar Kanitkar, Junior, EECS, UC Berkeley (January - December 2007)
- Wenchao Li, Senior, EECS, UC Berkeley (June 2006 - May 2007)
- Timothy Washington, Junior, CIS, Clark Atlanta University, SUPERB-IT participant (June - August 2006)
- Yinmeng N. Zhang, Junior, Computer Science, CMU (September 2004 - May 2005)
- Andrew P. Lin, Senior, Mathematical Sciences, CMU (May 2003 - April 2004)

Ph.D. Qualifying Exam / Dissertation Committees

Adam Chlipala (EECS, UC Berkeley, Apr. 2006), Donald Chai (EECS, UC Berkeley, May 2006), David Molnar (EECS, UC Berkeley, May 2006), Wei Zheng (EECS, UC Berkeley, Oct. 2006), Michael Case (EECS, UC Berkeley, May 2007), Nathan Kitchen (EECS, UC Berkeley, May 2007), Guoqiang Wang (EECS, UC Berkeley, May 2007), Haibo Zeng (EECS, UC Berkeley, May 2007), Thomas Feng (EECS, UC Berkeley, Jan. 2008), Armando Solar-Lezama (EECS, UC Berkeley, Feb. 2008), Mark Whitney (EECS, UC Berkeley, Mar. 2008), Gilad Arnold (EECS, UC Berkeley, Mar. 2008), Matthew Moskevicz (EECS, UC Berkeley, Feb. 2009), Yang Yang (EECS, UC Berkeley, Oct. 2009), Shanna-Shaye Forbes (EECS, UC Berkeley, Dec. 2010), Sayak Ray (EECS, UC Berkeley, April 2011).

M.S. Dissertation Committees

Thomas Feng (EECS, UC Berkeley, Fall 2008), Shanna-Shaye Forbes (EECS, UC Berkeley, Spring 2009), Jeff Jensen (EECS, UC Berkeley, Fall 2009), Cynthia Sturton (EECS, UC Berkeley, Fall 2010).

University Service

At UC Berkeley:

- 2010-12 Member, EECS Undergraduate Study Committee
- 2011-12 Member, EECS Student Awards Committee
- 2005-11 Member, EECS Graduate Admissions/Advising Committee
- 2006-11 Member, Preliminary Examination Committee in Computer-Aided Design for VLSI
- 2010-11 Member, College of Engineering ABET Preparation Committee
- 2006-12 Undergraduate Advising, EECS Department

Elsewhere:

- 2000-03 Co-organizer, SCS Student Seminar Series, a forum at CMU in which students from all areas of Computer Science and Engineering participated.
- 1996-97 Technical Co-ordinator, Computer Science and Engineering Association, IIT Bombay. Conducted city-wide technical workshops.

Professional Activities and Service

Memberships: ACM, IEEE, IEEE Computer Society, Sigma Xi.

Editorial Boards and Conference Committees:

- Associate Editor, IEEE Embedded Systems Letters (12/2008 - 12/2010)
 - co-edited special issue on Automotive Embedded Systems (March-May, 2010)
- Program co-chair, 24th International Conference on Computer-Aided Verification (CAV), 2012.

- Chair of Verification track and Member of Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2010 & 2011.
- Program co-chair, 9th International Workshop on Satisfiability Modulo Theories (SMT), 2011.
- Program co-chair, 1st Workshop on Quantitative Analysis of Software (QA), 2009.
- Member, Program Committee, 23rd International Conference on Computer-Aided Verification (CAV), 2011.
- Member, Program Committee, 3rd NASA Formal Methods Symposium, 2011.
- Member, Program Committee, International Conference on Embedded Software (EMSOFT), 2010.
- Member, Program Committee, ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), 2010.
- Member, Program Committee, Hardware Verification Workshop (HWVW), 2010.
- Member, Program Committee, 16th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2010.
- Member, Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2009.
- Member, Program Committee, 4th International Workshop on Automated Formal Methods (AFM), 2009.
- Member, Program Committee, International Conference on Formal Modelling and Analysis of Timed Systems (FORMATS), 2009.
- Member, Program Committee, 21st International Conference on Computer-Aided Verification (CAV), 2009.
- Member, Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2008.
- Member, Program Committee, IJCAR '08 Workshop on Practical Aspects of Automated Reasoning (PAAR), 2008.
- Member, Best Paper Award Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2007.
- Member, Program Committee, 18th International Conference on Computer-Aided Verification (CAV), 2006.

Reviewing Grant Proposals: (2006-10)

- National Science Foundation Panels.
- Israel-U.S. Binational Science Foundation, Austrian Science Foundation.

Reviewing Journal and Conference Articles: (apart from program committee and editorial board service)

Journals: Journal of the ACM, Proceedings of the IEEE, ACM Transactions on Computational Logic, ACM Transactions on Design Automation of Electronic Systems, Acta Informatica, Constraints, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Computers, Formal Aspects of Computing, Journal of AI Research, Journal of Symbolic Computation.

Conferences: Computer-Aided Verification (CAV 2001, 2004, 2008), Computer Science Logic (CSL 2002), Design Automation and Test in Europe (DATE 2004), Formal Methods in Computer-Aided Design (FMCAD 2002 & 2004), Foundations of Software Technology and Theoretical Computer Science (FSTTCS 2000 & 2002) ACM/IEEE International Conference on Mobile Computing and Networking (MOBICOM 2000), ACM SIGCOMM (2002), Tools and Algorithms for the Construction and Analysis of Systems (TACAS 2004, 2005, 2006, 2008).

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