

An Efficient Data Transmission Interface for VLSI Systems using Code-Division Multiple Access Technique

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Abstract

An efficient data transmission bus interface for VLSI systems is proposed. Unlike its predecessors, the proposed MB-CDMA (Multiple-Bit Code Division Multiple Access) bus is capable of transmitting multiple-bit data at each cycle. All signals transmitted through the MB-CDMA bus are modulated using Pseudo-Noise sequence codes, enabling parallel transmissions using the same bus line. Due to its narrow band rejection features, the voltage swing at the bus can be reduced to tens of milli-volts to achieve low power consumption. The MB-CDMA interface had been successfully implemented with a $0.6\mu\text{m}$ CMOS process.

1. Introduction

Code Division Multiple Access (CDMA) technique is popular in wireless communication systems for its narrow-band noise rejection features [1]. By introducing the CDMA technique into a bus, we managed to reduce the signal swing on the bus to ten of milli-volts in order to cut down power consumption [2]. This is achieved without sacrificing the noise margin because of demodulation at the CDMA interface receivers. Theoretically, the transmission capability of both TDMA bus and CDMA bus should be similar. However, as MB-CDMA bus interface proposed in this paper is designed for multiple bit transmission, the capability of the bus increase significantly.

2. MB-CDMA Transmission Technique

Figure 1 illustrates the differences between TDMA and CDMA techniques. In TDMA, transmitting time is divided into many smaller time slot that is used as a communication channel. In contrast, CDMA utilizes PN code as communication channel. Consequently, CDMA poses wider bandwidth compared to TDMA because the frequencies are spread out by using Pseudo Noise (PN) sequence codes. One benefit of spreading the signal in the frequency domain is that a signal with wider bandwidth is less suscep-

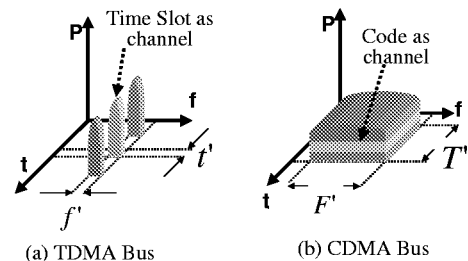


Figure 1. CDMA vs TDMA

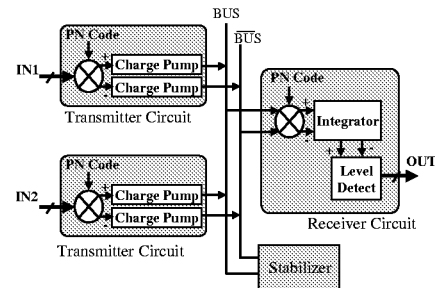


Figure 2. Block diagram of MB-CDMA bus interface

tible to degradation from narrow-band noise. The CDMA technique used in this work is a simplified version from those used in wireless telecommunication systems. A global clock is utilized to ensure synchronization of all component circuits. In addition, PN codes used in this work are the M-sequence codes with an extra bit added. The additional bit is to ensure high self-correlation and zero correlation between any two sequence codes. This feature of the PN code is important because it enables multiple bit data transmission.

Figure 2 depicts the block diagram of MB-CDMA interface that consists of transmitters, receivers and a stabilizer. At the transmitters, the data will be modulated with a PN code. The modulated signals will be then injected into the CDMA bus through charge pump circuit. Signal swing at the bus should be proportional to the data being sent but it is kept small. This is illustrated in Fig. 3. Due to the random nature and high frequency of the PN code, the modulated data spectrum has a wider bandwidth than the original signal. By detecting the level of receiver's output,

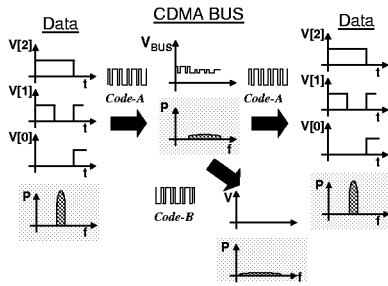


Figure 3. MB-CDMA Technique

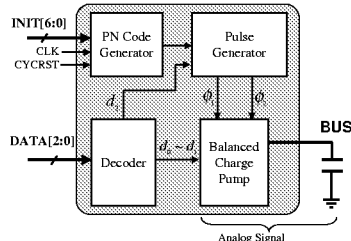


Figure 4. Transmitter Circuit

all the transmitted data will be received. The signal will be restored only if the same PN code is used for demodulation at the receivers, because correlation between the two different PN codes is zero.

Therefore, assignment of the same PN code for both the transmitters and the receivers correspond to a virtual direct connection of their digital data streams. These connections do not require numerous interconnections, but they are flexible and re-programmable even during system operation. In addition, although the signal on the bus looks like analog with discrete voltage steps, the input of the transmitter and the output of the receiver are conventional digital signals, indicating compatibility with a conventional digital bus.

3. Transmitter Circuit

Figure 4 depicts block diagram of the transmitter in MB-CDMA interface which consists of a PN code generator, a control pulse generator, a decoder and a balanced charge pump circuit. The extra bit is added during the reset phase of each clock cycle. The circuit illustrated in this paper transmits 3-bits of data concurrently. However, note that this number can be increased using the same architecture but with higher precision circuit. PN code generator consists of a linear feedback shift register (LFSR) as shown in Fig. 5. The PN code length used in MB-CDMA interface is 128. LFSR generates M-sequence PN codes [3] and by resetting the registers at the end of each clock cycle, an extra bit is added. The output of PN code generator is then used to modulate the transmission circuit using control pulse generator and the balanced charge pump circuit. The control pulse generator and decoder control the amount of charge (Q_c) injected to

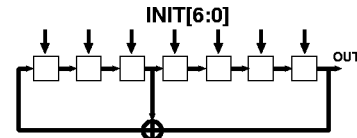


Figure 5. Linear Feedback Shift Registers - Generating 127 types of code depending on INIT[6:0]

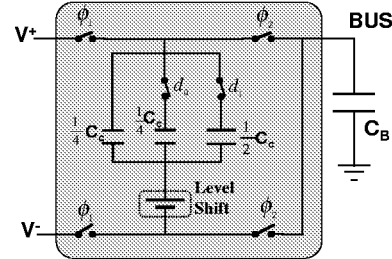


Figure 6. Charge pump circuit

the differential bus in accordance to the data resulting the voltage swing as shown in Table 1.

Figure 6 shows the balanced charge pump circuit proposed for the CDMA bus interface [4]. The amount of charge injected by the balanced charge pump circuit is independent of the bus voltage and the effects of parasitic capacitance or mismatch can be kept low. Depending on the transmitting data, charging capacitance switches between $1/4C_c$, $1/2C_c$, $3/4C_c$ and C_c which contributed to the peak-to-peak voltage swing $15mV$, $30mV$, $45mV$ and $60mV$ respectively. MSB of the data is represented by the polarity of the charge as shown in Table 1.

Simulation results using only one transmitter is shown in Fig. 3. The voltage swing changes in accordance to transmitting data sequence, $\{7,6,5,4,3,2,1,0\}$. The smaller graph depicts the voltage of multiple access bus for one transmitting cycle. Note that the behavior of the bus is similar to the PN code except that the voltage swing is much reduced.

Power consumption on the bus line per every 3-bit data transmission for MB-CDMA and conventional TDMA based CMOS architecture are as shown in Eqn. 1, where n is the PN code length and f as frequency. As δV is much smaller compared to voltage

Table 1. Corresponding charges and voltage swing to input data

Data	Charge (Q_c)	Voltage Swing(Q_c/C_{BUS})
3'b111	$1/4C_c(V^+ - V^-)$	$60mV$
3'b110	$1/2C_c(V^+ - V^-)$	$45mV$
3'b101	$3/4(V^+ - V^-)$	$30mV$
3'b100	$C_c(V^+ - V^-)$	$15mV$
3'b011	$-1/4C_c(V^+ - V^-)$	$-60mV$
3'b010	$-1/2C_c(V^+ - V^-)$	$-45mV$
3'b001	$-3/4C_c(V^+ - V^-)$	$-30mV$
3'b000	$-C_c(V^+ - V^-)$	$-15mV$

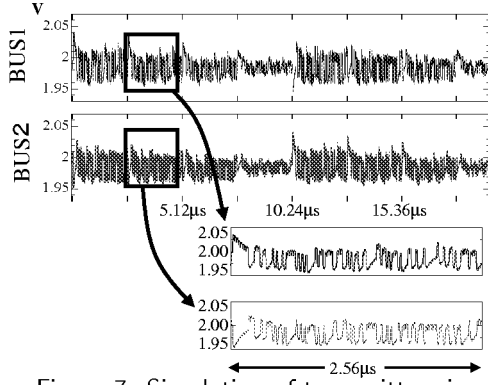


Figure 7. Simulation of transmitter circuit

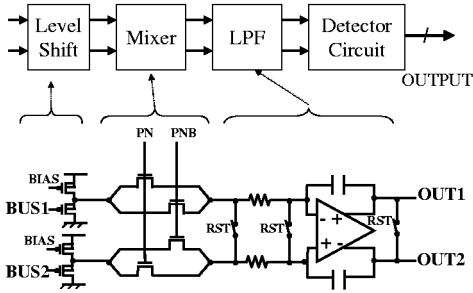


Figure 8. Receiver circuit

swing in most TDMA bus, the power consumption on the bus for MB-CDMA is much smaller.

$$P_{CDMA} = \frac{f}{2} C (\delta V)^2 \times n \quad (1)$$

$$P_{TDMA} = \frac{f}{2} C V^2 \times 3 \quad (2)$$

4. Receiver Circuit

The receiver circuit as shown in Fig. 8 has a CMOS double-balanced mixer to demodulate the signal on the bus by PN code. As the bus line cannot be connected directly to the mixer, a level shift is inserted. The demodulated signal will be then integrated over for one transmitting cycle using a low pass filter, before being connected to a detector circuit. If signals transmitted through modulation using the same PN code do not exist, the output of the LPF stays in a limited range (less than V_{ref1}), because the mixer does not detect much correlation. Should the demodulation PN code matches the transmitting PN code,

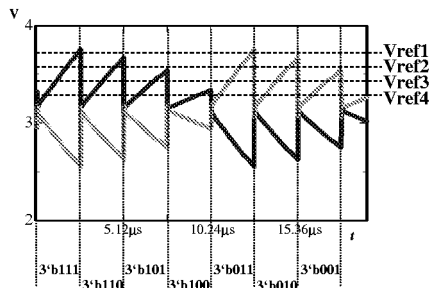


Figure 9. Simulation of receiver circuit demodulating transmitting data shown in Fig. 7

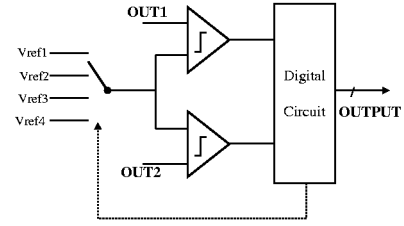


Figure 10. Detector circuit

the output of LPF will increase or decrease linearly as shown in Fig. 9. The voltage level of LPF output is proportional to the data transmitted. At the end of each transmitting cycle, the circuit will be reset through RST shown in Fig. 8.

Table 2. Corresponding output of detector circuit to reference voltage

Conditions	Data Detected
$V_{OUT1}, V_{OUT2} < V_{ref1}$	No Signal
$V_{ref1} < V_{OUT1} < V_{ref2}$	3'b100
$V_{ref2} < V_{OUT1} < V_{ref3}$	3'b101
$V_{ref3} < V_{OUT1} < V_{ref4}$	3'b110
$V_{OUT1} > V_{ref4}$	3'b111
$V_{ref1} < V_{OUT2} < V_{ref2}$	3'b000
$V_{ref2} < V_{OUT2} < V_{ref3}$	3'b001
$V_{ref3} < V_{OUT2} < V_{ref4}$	3'b010
$V_{OUT2} > V_{ref4}$	3'b011

Figure 9 shows simulation results of LPF output voltage when the receiver is connected to the bus which carries the transmitted data shown in Fig. 7. The output of LPF is connected to a detector circuit as shown in Fig. 10 which consists of two comparators and a digital circuit block. At the initial stage, the comparators are connected to V_{ref1} but when the one of the LPF output becomes larger, the reference voltage is switched to V_{ref2} and the event continues. The relation between LPF output and the reference circuit is as shown in Table 2.

5. Stabilizer Circuit

To keep the DC level of the bus line voltage around the bias point, a stabilizer circuit having a LPF with a reference voltage is implemented as shown in Fig. 11. At the end of each clock cycle, the two differential bus will be shorted while being connected directly to

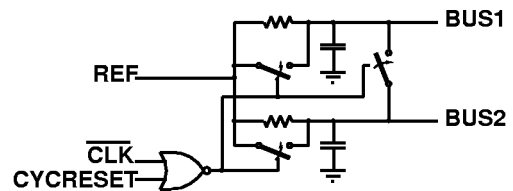


Figure 11. Stabilizer circuit

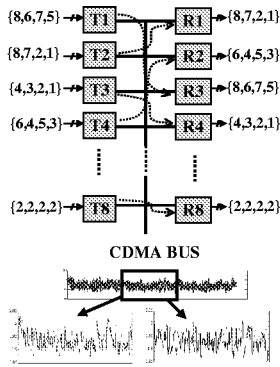


Figure 12. Simulation of 8 pairs of transmitter and receiver circuits

the reference voltage so that the charge on the bus will be redistributed. During data transmission, the stabilizer functions as a LPF which stabilize the bus line, getting rid of low frequency noise.

6. Simulation Results

The proposed MB-CDMA bus interface had been implemented using a $0.6\mu\text{m}$, double-poly triple-metal CMOS process. The prototype chip consists of eight pairs of transmitters and receivers. Figure 12 shows simulation results of whole circuit operation for eight-to-eight ports communication. The results demonstrate that the new bus interface operate correctly even with a small amplitude voltage step of 60mV at bus lines. Theoretically, the number of parallel transmission allowed on the bus is half of the PN code length (64). The multiple access bus resembles noise-like signals because it is the sum of eight Pseudo Noise (PN) codes. Large voltage swing signals have no effect on the lower voltage swing signals because they are eliminated through demodulation.

7. Features of MB-CDMA Bus

1. Low Power Consumption for Bus Line : Compared to conventional TDMA bus at the same bandwidth in which full swing is applied, the proposed MB-CDMA bus has lower power consumption due to its low voltage swing. This is achieved without the sacrificing of the noise margin. As illustrated in Fig. 13, noise margin of MB-CDMA is maintained at 100mV , much larger than the

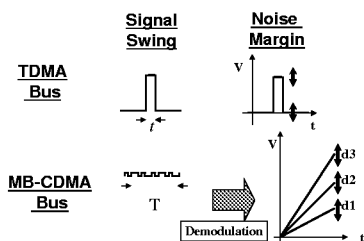


Figure 13. MB-CDMA vs TDMA

signal swing on the bus which is impossible to achieve in TDMA based tri-state bus.

2. Noise Tolerance : The MB-CDMA rejects narrow band noise. In addition, the differential bus used is capable of rejecting common mode white noise.
3. Parallel Transmission of Data : Unlike TDMA bus, all signals are transmitted in parallel. Moreover, with its simple programmability by assigning PN codes to establish communication channels, MB-CDMA bus is suitable for parallel processing systems.
4. Multiple Bit Transmission per Channel : Each communication channel can transmit multiple bits of data simultaneously. Compared to its predecessors, transmission rate of MB-CDMA is 3 times faster because it transmitted multiple bits simultaneously.

8. Conclusions and Future Work

A new bus interface in which multiple bit of data can be transmitted in parallel has been proposed. The new bus architecture features low power consumption, noise tolerance and dynamical programmability and it is suitable for parallel processing systems. Circuit implementation of transmitters and receivers has been discussed. We have also verified the feasibility of the MB-CDMA bus architecture through VLSI implementation of eight pairs of transmitters and receivers. However, the limitation of the proposed circuit in term of speed has yet to be explored.

9. Acknowledgement

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