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Education

1985 B.S. and M.S. in Computer Science, Massachusetts Institute of Technology
1991 Ph.D. in Computer Science, Massachusetts Institute of Technology

Experience

University of California, Berkeley (1991-present)

Professor, Computer Science (2002-present)
Associate Professor, Computer Science (1996-present)
Assistant Professor, Computer Science (1991-1996)

Lawrence Berkeley National Laboratory (1996-present)

Faculty Research Scientist (1996-present)
Future Technologies Group Lead (2005-present)

ETH, Zurich, Switzerland (Summer, 1996)

Visiting Researcher

Massachusetts Institute of Technology (Fall, 1996)

Visiting Associate Professor

Clark University (Spring, 1985)

Visiting Instructor

Awards

- Best Student Paper Award, Rewriting Techniques and Applications, 1985.
- Teaching award with promotion to Instructor ``G'' from EECS Department at MIT, 1987.
- George M. Sprowls Award for Best PhD Dissertation, EECS Department at MIT, 1991.
- ARO Young Investigator Award, 1996.
- Computer Science Division Diane S. McEntyre Award for Excellence in Teaching, U.C. Berkeley, 2001.
- Best Student Paper Award, ICS 2002: Workshop on Performance Optimization via High-Level Languages and Libraries.
- Best Paper Award, International Conference on Parallel Processing, 2004.
- Okawa Foundation Research Grant 2005.
- HPCWire "People to Watch" 2006.
- Best Paper Award, International Parallel and Distributed Processing Symposium, 2008.
- National Academies, National Research Council Committee on "Sustaining Growth in Computing Performance," 2007-2009.

Publications

Books

- [1] "Assessment of High-End Computing Research and Development in Japan," Al Trivelpiece, Rupak Biswas, Jack Dongarra, Peter Paul, Katherine Yelick, World Technology Evaluation Center, Inc., 2004. Available from <http://www.wtec.org/reports.htm>.

- [2] "UPC: Distributed Shared-Memory Programming," Tarek El-Ghazawi, William Carlson, Thomas Sterling, and Katherine Yelick, Wiley-Interscience, May 2005.

Refereed Journal and Conference Papers

- [3] Sam Williams, Kaushik Datta, Jonathan Carter, Leonid Oliker, John Shalf, Katherine Yelick, David Bailey, PERI - Auto-tuning Memory Intensive Kernels for Multicore, SciDAC: Scientific Discovery Through Advanced Computing, Seattle Washington, July, 2008. Journal of Physics: Conference Series. LBNL # pending. To appear.
- [4] Kaushik Datta, Shoaib Kamil, Sam Williams, Leonid Oliker, John Shalf, Katherine Yelick, "Optimization and Performance Modeling of Stencil Computations on Modern Microprocessors", SIAM Review. LBNL-63192. To appear.
- [5] Kaushik Datta, Mark Murphy, Vasily Volkov, Samuel Williams, Jonathan Carter, Leonid Oliker, David Patterson, John Shalf, and Katherine Yelick, "Stencil Computation Optimization and Autotuning on State-of-the-Art Multicore Architectures," Proceedings of the ACM/IEEE Conference on Supercomputing (SC08), November 2008. LBNL # Pending. To appear.
- [6] S. W. Williams, D. A. Patterson, L. Oliker, J. Shalf, K. Yelick, "The Roofline Model: A pedagogical tool for auto-tuning kernels on multicore architectures", HOT Chips, A Symposium on High Performance Chips, Stanford, CA, Aug 2008. (Abstract.)
- [7] Costin Iancu, Wei Chen, Katherine A. Yelick: Performance portable optimizations for loops containing communication operations. International Conference on Supercomputing (ICS), Island of Kos, Greece, June 7-12, 2008, pages 266-276.
- [8] J. Demmel, M. Hoemmen, M. Mohiyuddin, K. Yelick, "Avoiding Communication in Sparse Matrix Computations," IEEE Intern. Parallel and Distributed Processing Symposium (IPDPS'08), April 2008.
- [9] Samuel Williams, Jonathan Carter, Leonid Oliker, John Shalf, Katherine Yelick, "Lattice Boltzmann Simulation Optimization on Leading Multicore Platforms," IEEE International Parallel and Distributed Processing Symposium (IPDPS'08), April 2008. **Best Paper Award**, Applications Track.
- [10] John Mellor-Crummey, Peter Beckman, Jack Dongarra, Ken Kennedy, Barton Miller, Katherine Yelick. "Software for leadership-class computing," SciDAC Review. Fall 2007, pages 36-45.
- [11] Jimmy Su and Katherine Yelick, "Automatic Performance Debugging in Partitioned Global Address Space Programs" 20th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Urbana, Illinois, October 2007. Lecture Notes in Computer Science 5234 Springer 2008, ISBN 978-3-540-85260-5.
- [12] Parry Husbands and Katherine Yelick, "Multithreading and One-Sided Communication in Parallel LU Factorization." Proceedings of Supercomputing (SC07), Reno, NV, November, 2007.
- [13] Tong Wen, Jimmy Su, Phillip Colella, Katherine Yelick and Noel Keen, "An Adaptive Mesh Refinement Benchmark for Modern Parallel Programming Languages." Proceedings of Supercomputing (SC07), Reno, NV, November 2007.
- [14] Sam Williams, Leonid Oliker, Richard Vuduc, John Shalf, Katherine Yelick, James Demmel, "Optimization of Sparse Matrix-Vector Multiplication on Emerging Multicore Platforms." Proceedings of Supercomputing (SC07), November 2007.
- [15] Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands, and Katherine Yelick, "Scientific Computing Kernels on the Cell Processor," International Journal of Parallel Programming. To appear.
- [16] Amir Kamil and Katherine Yelick, "Hierarchical Pointer Analysis for Distributed Programs," Static Analysis Symposium (SAS), Kongens Lyngby, Denmark, August 22-24, 2007.
- [17] Katherine Yelick, Paul Hilfinger, Susan Graham, Dan Bonachea, Jimmy Su, Amir Kamil, Kaushik Datta, Phillip Colella, and Tong Wen, "Parallel Languages and Compilers: Perspective from the Titanium Experience." Journal of High Performance Computing Applications, August 2007, vol. 21, pp. 266-290.
- [18] K. Yelick, D. Bonachea, W.-Y. Chen, P. Colella, K. Datta, J. Duell, S. Graham, P. Hargrove, P. Hilfinger, P. Husbands, C. Iancu, A. Kamil, R. Nishtala, J. Su, M. Welcome, T. Wen, "Productivity and Performance Using Partitioned Global Address Space Languages," Proceedings of Parallel Symbolic Computation (PASC0), London, Ontario, July 27-28, 2007.
- [19] Alfredo Buttari, Jack Dongarra, Parry Husbands, Jakub Kurzak and Katherine Yelick, "Multithreading for synchronization tolerance in matrix factorization," Proceedings of the SciDAC 2007 Conference, Boston,

- Massachusetts, July 24-28, 2007. Published in the Journal of Physics: Conference Series. Volume 78, 2007, June, 2007.
- [20] Wei Chen, Dan Bonachea, Costin Iancu, and Katherine Yelick, "Automatic Nonblocking Communication for Partitioned Global Address Space Programs," Proceedings of the International Conference on Supercomputing (ICS), Seattle, Washington, June 16-17, 2007.
 - [21] Shivali Agarwal, Rajkishore Barik, Dan Bonachea, Vivek Sarkar, Rudrapatna Shyamasundar, Katherine Yelick, "Deadlock-Free Scheduling of X10 Computations with Bounded Resources," Symposium on Parallel Algorithms and Architecture (SPAA), San Diego California, June 9-11, 2007.
 - [22] Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands, and Katherine Yelick, "Scientific Computing Kernels on the Cell Processor," International Journal of Parallel Programming (IJPP), DOI 10.1007/s10766-007-0034-5, April 2007.
 - [23] Ewing Lusk and Katherine Yelick, "Languages for High-Productivity Computing: The DARPA HPCS Language Project," Parallel Processing Letters, Vol. 17, No. 1, March 2007, pp. 89-102.
 - [24] Rajesh Nishtala, Richard Vuduc, James Demmel, and Katherine Yelick, "When Cache Blocking Sparse Matrix Multiply Works and Why." Applicable Algebra in Engineering, Communication and Computing, March 2007.
 - [25] Hormozd Gahvari, Mark Hoemmen, James Demmel, Katherine Yelick, "Benchmarking Sparse Matrix-Vector Multiply in Five Minutes," SPEC Benchmark Workshop 2007, Austin, TX, January 2007.
 - [26] Hongzhang Shan, Erich Strohmaier, Ji Qiang, David H. Bailey, and Kathy Yelick, "Performance Modeling and Optimization of a High Energy Colliding Beam Simulation Code," Proceedings of SC2006, Nov 2006. Also appeared as Lawrence Berkeley National Laboratory Technical Report, LBNL-60180.
 - [27] Shoaib Kamil, Kaushik Datta, Sam Williams, Leonid Oliker, John Shalf, Katherine Yelick, "Implicit and Explicit Optimizations for Stencil Computations," ACM Workshop on Memory Systems Performance and Correctness, San Jose, California, October 22, 2006.
 - [28] Katherine Yelick, "Performance Advantages of Partitioned Global Address Space Languages," Recent Advances in Parallel Virtual Machine and Message Passing Interface, Lecture Notes in Computer Science, Springer Berlin / Heidelberg, Volume 4192/2006, September 21, 2006. (Short abstract only.)
 - [29] Edward Givelberg, Katherine Yelick, "Distributed Immersed Boundary Simulations in Titanium." SIAM Journal on Scientific Computing, Volume 28 Issue 4, Pages 1361-1378, August 7, 2006.
 - [30] Sam Williams, John Shalf, Leonid Oliker, Parry Husbands, Shoaib Kamil, Katherine Yelick, "The Potential of the Cell Processor for Scientific Computation," ACM International Conference on Computing Frontiers, Ischia, Italy, May 2-5, 2006.
 - [31] Christian Bell, Dan Bonachea, Rajesh Nishtala, and Katherine Yelick, "Optimizing Bandwidth Limited Problems Using One-Sided Communication and Overlap," 20th International Parallel & Distributed Processing Symposium (IPDPS), Rhodes Island, Greece, April 25-29, 2006. Also available as Lawrence Berkeley National Lab Tech Report LBNL-59207.
 - [32] Eun-Jin Im, Ismail Bustany, Cleve Ashcraft, James W. Demmel, and Katherine A. Yelick "Performance Tuning of Matrix Triple Products Based on Matrix Structures," Springer Lecture Notes in Computer Science, Applied Parallel Computing: State of the Art in Scientific Computing: Revised Selected Papers from the 7th International Workshop, PARA 2004 Lyngby, Denmark, June 20-23, 2004; Springer-Verlag New York Inc, March 15, 2006, pp. 740-746.
 - [33] Amir Kamil, Jimmy Su, and Katherine Yelick, "Making Sequential Consistency Practical in Titanium." Supercomputing 2005 (SC05), Seattle, Washington, November 2005.
 - [34] Amir Kamil and Katherine Yelick, "Concurrency Analysis for Parallel Programs with Textually Aligned Barriers." 18th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Hawthorne, New York, October 2005.
 - [35] Kaushik Datta, Dan Bonachea and Katherine Yelick. "Titanium Performance and Potential: an NPB Experimental Study." 18th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Hawthorne, New York, October 2005.
 - [36] Wei-Yu Chen, Costin Iancu, and Katherine Yelick, "Communication Optimizations for Fine-grained UPC Applications," 14th International Conferences on Parallel Architectures and Compilation Techniques (PACT '05), St. Louis, MO, Sept. 17-21, 2005.
 - [37] J. Demmel, K. Yelick, and R. Vuduc. "OSKI: An Automatically Tuned Library of Sparse Matrix Kernels." Proceedings of SciDAC Conference 2005, Scientific Discovery through Advanced Computing, 26-30 June 2005, San Francisco, CA, USA. Published in the Journal of Physics: Conference Series, Volume 16, 2005.

- [38] S. Kamil, P. Husbands, J. Shalf, L. Oliker, K. Yelick, "Impact of Modern Memory Subsystems on Cache Optimizations for Stencil Computations," 3rd Annual ACM SIGPLAN Workshop on Memory Systems Performance, June 2005.
- [39] J. Demmel, J. Dongarra, V. Eijkhout, E. Fuentes, A. Petitet, R. Vuduc, R. C. Whaley, K. Yelick, "Self-Adapting Linear Algebra Algorithms and Software." Proceedings of the IEEE, Special Issue on Program Generation, Optimization, and Adaptation, vol. 93, no. 2, February 2005.
- [40] J. Su and K. Yelick, "Automatic Support for Irregular Computations in a High-Level Language," 19th International Parallel and Distributed Processing Symposium (IPDPS), Denver, Colorado, April 2005.
- [41] M. Narayanan and K. Yelick, "Generating permutation instructions from a high level description." 6th Workshop on Media and Streaming Processors, Portland, Oregon, December 5, 2006.
- [42] B. Lee, R. Vuduc, J. Demmel, K. Yelick, "Performance Models for Evaluation and Automatic Tuning of Symmetric Sparse Matrix-Vector Multiply," *International Conference on Parallel Processing*, Montreal, Quebec, Canada, August 2004. Winner, **Best Paper Award**.
- [43] C. Bell, W. Chen, D. Bonachea, and K. Yelick, "Evaluating Support for Global Address Space Languages on the Cray X1." International Conference on Supercomputing (ICS'04), Saint-Malo, France, June 2004.
- [44] J. Su and K. Yelick, "Array Prefetching for Irregular Array Accesses in Titanium" 6th International Workshop on Java[™] for Parallel and Distributed Computing, Santa Fe, New Mexico, April 2004.
- [45] G. Griem, L. Oliker, J. Shalf, and K. Yelick, "Identifying Performance Bottlenecks on Modern Microarchitectures using an Adaptable Probe," Workshop on Performance Modeling, Evaluation, and Optimization of Parallel and Distributed Systems, Santa Fe, New Mexico, April 2004. Also appeared as LBNL Technical Report 54901.
- [46] E.-J. Im, K. Yelick, and R. Vuduc, "SPARSITY: An Optimization Framework for Sparse Matrix Kernels." International Journal of High Performance Computing Applications, 18 (1), pp. 135-158, 2004.
- [47] Wei-Yu Chen, Arvind Krishnamurthy, Katherine Yelick, "Polynomial-time Algorithms for Enforcing Sequential Consistency in SPMD Programs with Arrays," 16th International Workshop on Languages and Compilers for Parallel Computing (LCPC), College Station, Texas, October 2003.
- [48] W. Chen, D. Bonachea, J. Duell, P. Husbands, C. Iancu, K. Yelick, "A Performance Analysis of the Berkeley UPC Compiler," 17th Annual International Conference on Supercomputing (ICS), San Francisco, California, June 2003.
- [49] Richard Vuduc, Attila Gyulassy, James W. Demmel, Katherine A. Yelick, "Memory Hierarchy Optimizations and Performance Bounds for Sparse $A^T A * x$," ICCS 2003: Workshop on Parallel Linear Algebra. Melbourne, Australia, June 2003.
- [50] C. Bell, D. Bonachea, Y. Cote, J. Duell, P. Hargrove, P. Husbands, C. Iancu, M. Welcome, K. Yelick, "An Evaluation of Current High Performance Networks," International Parallel and Distributed Processing Symposium, Nice, France, April 22-26, 2003.
- [51] R. Vuduc, J. Demmel, K. Yelick, S. Kamil, R. Nishtala, B. Lee. "Performance Optimizations and Bounds for Sparse Matrix-Vector Multiply." Proceedings of the IEEE/ACM Conference on High Performance Computing and Communications ("Supercomputing"), SC02, Baltimore, November, 2002.
- [52] R. Vuduc, S. Kamil, J. Hsu, R. Nishtala, J. Demmel, K. Yelick. "Automatic Performance Tuning and Analysis of Sparse Triangular Solve." ICS 2002: Workshop on Performance Optimization via High-Level Languages and Libraries, New York, June 22, 2002. **Best Student Paper and Best Student Presentation..**
- [53] Brian R. Gaeke, Parry Husbands, Xiaoye S. Li, Leonid Oliker, Katherine A. Yelick, and Rupak Biswas. "Memory-Intensive Benchmarks: IRAM vs. Cache-Based Machines," Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS). Ft. Lauderdale, FL. April, 2002.
- [54] D. Oppenheimer, A. Brown, J. Beck, D. Hettena, J. Kuroda, N. Treuhaft, D.A. Patterson, and K. Yelick, "ROC-1: Hardware Support for Recovery-Oriented Computing." IEEE Transactions on Computers, vol. 51, no. 2, pp. 100-107, Feb. 2002. Special Issue on Embedded Fault-Tolerant Computer Systems.
- [55] Christoforos Kozyrakis, David Judd, Joeseeph Gebis, Samuel Williams, David Patterson, Katherine Yelick, "Hardware/compiler Codevelopment for an Embedded Media Processor," *Proceedings of the IEEE*, vol. 89, no. 11, pages 1694-1709, November 2001.
- [56] E.-J. Im and K. Yelick, "Optimizing Sparse Matrix Computations for Register Reuse in Sparsity," Proceedings of the International Conference on Computational Science, San Francisco, May 2001.
- [57] E.-J. Im and K. Yelick, "Optimization of Sparse Matrix Kernels for Data Mining," Proceedings of Text Mine Workshop '01, Chicago, April 7, 2001.
- [58] D. Judd, K. Yelick, C. Kozyrakis, D. Martin, and D. Patterson, "Exploiting On-Chip Memory Bandwidth in the VIRAM Compiler," Second Workshop on Intelligent Memory Systems, Cambridge, November 2000.

- [59] T. Nguyen, A. Zakhor and K. Yelick, "Performance Analysis of an H.263 Video Encoder on VIRAM," International Conference on Image Processing (ICIP), Vancouver, B.C., Canada, September 2000.
- [60] R. H. Arpaci-Dusseau, E. Anderson, N. Treuhaft, D. E. Culler, J. M. Hellerstein, D. A. Patterson, and K. A. Yelick, "Cluster I/O with River: Making the Fast Case Common, Workshop on I/O in Parallel and Distributed Systems," Atlanta, GA, May 1999.
- [61] E. Im and K. A. Yelick, "Optimizing Sparse Matrix Vector Multiplication on SMPs," SIAM Conf. Parallel Processing for Scientific Computing, San Antonio, TX, March 1999.
- [62] E. Im and K. A. Yelick, "Model-based Memory Hierarchy Optimizations for Sparse Matrices," Workshop on Profile and Feedback-Directed Compilation, Paris, France, October 1998.
- [63] K. Yelick, L. Semenzato, G. Pike, C. Miyamoto, B. Liblit, A. Krishnamurthy, P. Hilfinger, S. Graham, D. Gay, P. Colella, and A. Aiken. "Titanium: A High-Performance Java Dialect," *Concurrency: Practice and Experience*, September-November 1998, pp. 825-36. Earlier version was presented at the ACM Workshop on Java for High-Performance Network Computing, February 1998.
- [64] S. Chakrabarti, J. Demmel, and K. Yelick. "Models and Scheduling Algorithms for Mixed Data and Task Parallel Programs." *Journal of Parallel and Distributed Computing*, Vol. 47, pp. 168--184. December 1997.
- [65] D. Patterson, K. Asanovic, A. Brown, R. Fromm, J. Golbus, B. Gribstad, K. Keeton, C. Kozyrakis, D. Martin, S. Perissakis, R. Thomas, N. Treuhaft, and K. Yelick. "Intelligent RAM (IRAM): the Industrial Setting, Applications, and Architecture." '97 International Conference on Compute Design, October 1997.
- [66] Kozyrakis, C.E., Perissakis, S., Patterson, D., Anderson, T., Asanovic, K., Cardwell, N., Fromm, R., Golbus, J., Gribstad, B., Keeton, K., Thomas, R., Treuhaft, N., Yelick, K. "Scalable processors in the billion-transistor era: IRAM," *Computer*, vol.30, (no.9), IEEE Comput. Soc, Sept. 1997. p.75-8.
- [67] R. Fromm, S. Perissakis, N. Cardwell, D. Patterson, T. Anderson, and K. Yelick. "The Energy Efficiency of IRAM Architectures." *Proceedings of the 24th Annual International Conference on Computer Architecture*, June 1997.
- [68] D. Patterson, T. Anderson, N. Cardwell, R. Fromm, K. Keeton, C. Kozyrakis, R. Thomas, and K. Yelick. "A Case for Intelligent DRAM: IRAM." *IEEE Micro*, April 1997, pp. 34--44. Also appeared as an Award Paper, *Hot Chips VIII*, August 1996.
- [69] D. Patterson, T. Anderson, N. Cardwell, R. Fromm, K. Keeton, C. Kozyrakis, R. Thomas, and K. Yelick. "Intelligent RAM (IRAM): Chips that remember and compute." *Proceedings of the 1997 IEEE International Solid-State Circuits Conference*, February 1997, pp. 224--225.
- [70] Krishnamurthy, K. E. Schausser, C. J. Scheiman, R. Y. Wang, D. E. Culler, and K. Yelick, "Evaluation of Architectural Support for Global Address-Based Communication in Large-Scale Parallel Machines." *Proceedings of Architecture Support on Programming Languages and Operating Systems*, 1996.
- [71] Krishnamurthy and K. Yelick, "Analyses and Optimizations for Shared Address Space Programs." *Journal of Parallel and Distributed Computation*, vol.38, (no.2), Academic Press, 1 Nov. 1996. pp.130--44.
- [72] S. Steinberg, J. Yang and K. Yelick, "Performance Modeling and Composition: A Case Study in Cell Simulation." *International Parallel Processing Symposium*, April 1996.
- [73] J. Jones and K. Yelick, "Parallelizing the Phylogeny Problem" *Supercomputing '95*, San Diego, California, December 1995.
- [74] C.-P. Wen and K. Yelick, "Portable Runtime Support for Asynchronous Simulation." *Proceedings of the International Conference on Parallel Processing*, Oconomowoc, Wisconsin, August 1995.
- [75] S. Chakrabarti, J. Demmel, and K. Yelick, "Modeling the Benefits of Mixed Data and Task Parallelism," *Proceedings of the Symposium on Parallel Algorithms and Architectures*, Santa Barbara, California, July 1995.
- [76] Krishnamurthy and K. Yelick, "Optimizing Parallel Programs with Explicit Synchronization." *Proceedings of the ACM Conference on Programming Language Design and Implementation (PLDI)*, San Diego, California, June 1995.
- [77] R. Arpaci, D. Culler, A. Krishnamurthy, S. Steinberg, and K. Yelick, "Empirical Evaluation of the CRAY-T3D: A Compiler Perspective," *International Symposium on Computer Architecture*, Santa Margherita Ligure, Italy, June 1995.
- [78] S.-T. Cheng, R. Brayton, G. York, K. Yelick, A. Saldana, "Compiling Verilog into Finite State Machines," *International Verilog Conference*, 1995.
- [79] S. Chakrabarti and K. Yelick, "Distributed Data Structures and Algorithms for Grobner Basis Computation," *Lisp and Symbolic Computation*, Volume 7, 1994, Pages 147--172.
- [80] Krishnamurthy and K. Yelick, "Optimizing Parallel SPMD Programs," *Workshop on Languages and Compilers for Parallel Computing*, August 1994.

- [81] S. Chakrabarti, A. Ranade, and K. Yelick, "Randomized Load Balancing for Tree Structured Computation," Scalable High Performance Computing Conference, Tennessee, May 1994.
- [82] C.-P. Wen and K. Yelick, "Compiling Sequential Programs for Speculative Parallelism," International Conference on Parallel and Distributed Systems, December 1993.
- [83] D. Culler, A. Dusseau, S. Goldstein, A. Krishnamurthy, S. Lumetta, T. von Eiken, and K. Yelick, "Parallel Programming in Split-C," Supercomputing '93, November 1993.
- [84] C.-P. Wen and K. Yelick, "Parallel Timing Simulation on a Distributed Memory Multiprocessor," International Conference on Computer Aided Design, November 1993.
- [85] S. Chakrabarti and K. Yelick, "On the Correctness of a Distributed Grobner Basis Algorithm," Proceedings of Rewriting Techniques and Applications, June 1993.
- [86] S. Chakrabarti and K. Yelick, "Implementing an Irregular Application on a Distributed Memory Multiprocessor," Principles and Practice of Parallel Programming, May 1993.
- [87] K. Yelick, "Programming Models for Irregular Applications," Workshop on Languages and Compilers and Run-Time Environments for Distributed Memory Multiprocessors, October 1992. Also appeared in SIGPLAN Notices, January 1993.
- [88] K. Yelick and S. J. Garland, "A Parallel Completion Procedure for Term Rewriting Systems," Conference on Automated Deduction, June 1992.
- [89] K. Yelick and J. Zachary, "Moded Type Systems for Logic Programming," Proceedings of the Sixteenth Annual ACM Symposium on Principles of Programming Languages, Austin, Texas, January 1989, pp. 116--124.
- [90] K. Yelick, "Unification in Combinations of Collapse-Free Regular Theories," Journal of Symbolic Computation, March 1987, pp. 153--181.
- [91] K. Yelick, "Combining Unification Algorithms for Confined Regular Equational Theories," Proceedings of the First International Conference on Rewriting Techniques and Applications, Dijon, Burgundy, France, Springer-Verlag, LNCS 202, May 1985, pp. 365--380. **Best Student Paper Award.**
- [92] Krishnamurthy, S. Lumetta, D. Culler, and K. Yelick "Connected Components on Distributed Memory Machines," Parallel Algorithms, DIMACS Series in Discrete Mathematics and Theoretical Computer Science, American Mathematical Society, 1997. (Also the proceedings of the 3rd DIMACS Parallel Implementation Challenge Workshop, October 1994.)
- [93] C.-P. Wen, S. Chakrabarti, E. Deprit, A. Krishnamurthy and K. Yelick, "Runtime Support for Portable Distributed Data Structures," Languages, Compilers and Run-Time Systems for Scalable Computers, (Proceedings 3rd Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers, Troy, NY, USA, May 1995.) Norwell, MA, USA: Kluwer Academic Publishers, 1996. pp. 111--120.
- [94] J. Zachary and K. Yelick, "Using Moded Type Systems to Support Abstraction in Logic Programs," Types in Logic Programming, F. Pfenning, editor, MIT Press, 1992.

Non-refereed Reports

- [95] Peter M. Kogge, Keren Bergman, Shekhar Borkar, William W. Carlson, William J. Dally, Monty Denneau, Paul D. Franzon, Stephen W. Keckler, Dean Klein, Robert F. Lucas, Steve Scott, Allan E. Snavely, Thomas L. Sterling, R. Stanley Williams, Katherine A. Yelick, William Harrod, Daniel P. Campbell, Kerry L. Hill, Jon C. Hiller, Sherman Karp, Mark A. Richards, Alfred J. Scarpelli, "Final Report of the Exascale Study Group: Technology Challenges in Achieving Exascale Systems." To Appear.
- [96] James Demmel, Mark Hoemmen, Marghoob Mohiyuddin, and Katherine Yelick, "Avoiding Communication in Computing Krylov Subspaces" University of California EECS Department Technical Report UCB/EECS-2007-123, October 2007.
- [97] John Mellor-Crummey, Peter Beckman, Jack Dongarra, Barton Miller, and Katherine Yelick, "Creating Software Technology to Harness the Power of Leadership-class Computing Systems," SciDAC Review 2007. To appear.
- [98] Richard Vuduc, James Demmel, and Katherine Yelick, "The Optimized Sparse Kernel Interface (OSKI) Library: User's Guide for Version 1.0.1h." Available from <http://bebop.cs.berkeley.edu>.
- [99] M. Narayanan and K. Yelick, "Generating permutation instructions from a high level description." Lawrence Berkeley National Laboratory Technical Report, LBNL-54900, December 2006.

- [100] Hongzhang Shan, Erich Strohmaier, Ji Qiang, David H. Bailey, and Kathy Yelick, "Performance Modeling and Optimization of a High Energy Colliding Beam Simulation Code," Lawrence Berkeley National Laboratory Technical Report LBNL-60180, 2006.
- [101] Christian Bell, Dan Bonachea, Rajesh Nishtala, and Katherine Yelick, "Optimizing Bandwidth Limited Problems Using One-Sided Communication and Overlap," Lawrence Berkeley National Laboratory, Computing Science Technical Report LBNL-59207, 2006. Available from: <http://www-library.lbl.gov/docs/LBNL/592/07/PDF/LBNL-59207.pdf>
- [102] S. Williams, J. Shalf, L. Oliker, P. Husbands, S. Kamil, and K. Yelick (2005). "The Potential of the Cell Processor for Scientific Computing." Lawrence Berkeley National Laboratory, Computing Sciences Technical Report LBNL-59071, 2006. Available from: <http://www-library.lbl.gov/docs/LBNL/590/71/PDF/LBNL-59071.pdf>
- [103] Krste Asanovic, Ras Bodik, Bryan Christopher Catanzaro, Joseph James Gebis, Parry Husbands, Kurt Keutzer, David A. Patterson, William Lester Plishker, John Shalf, Samuel Webb Williams and Katherine A. Yelick, "The Landscape of Parallel Computing Research: A View from Berkeley," EECS Department, University of California, Berkeley, Technical Report No. UCB/EECS-2006-183, December 18, 2006.
- [104] W. Chen, C. Iancu, and K. Yelick, "Communication Optimizations for Fine-Grained UPC Applications." Lawrence Berkeley National Laboratory Computing Science Technical Report LBNL-58382, 2005. Available from <http://www-library.lbl.gov/docs/LBNL/583/82/PDF/LBNL-58382.pdf>
- [105] The UPC Consortium, "The UPC Language Specifications, version 1.2." Lawrence Berkeley National Laboratory Technical Report, LBNL-59208, 2005.
- [106] P. Hilfinger, D. Bonachea, K. Datta, D. Gay, S. Graham, B. Liblit, G. Pike, J. Su and K. Yelick. "Titanium Language Reference Manual," U.C. Berkeley Tech Report, UCB/EECS-2005-15, 2005.
- [107] S. W. Williams, J. Shalf, L. Oliker, P. Husbands, and K. Yelick, "Dense and Sparse Matrix Operations on the Cell Processor," Lawrence Berkeley National Laboratory Technical Report LBNL-5825, 2005. Available from: <http://www-library.lbl.gov/docs/LBNL/582/53/PDF/LBNL-58253.pdf>
- [108] K. Yelick, S. Kamil, W. T. Kramer, L. Oliker, J. Shalf, H. Shan, and E. Strohmaier (2005). "Science Driven Supercomputing Architectures: Analyzing Architectural Bottlenecks with Applications and Benchmark Probes." Lawrence Berkeley National Laboratory, Technical Report LBNL-58914, 2005. Available from <http://www-library.lbl.gov/docs/LBNL/589/14/PDF/LBNL-58914.pdf>
- [109] Horst Simon, William T. C. Kramer, David H. Bailey, Michael J. Banda, E. Wes Bethel, Jonathon T. Carter, James M. Crow, William J. Fortney, John A. Hules, Nancy L. Meyer, Juan C. Meza, Esmond G. Ng, Lynn E. Rippe, William C. Saphir, Francesca Verdier, Howard A. Walter, Katherine A. Yelick, "Science Driven Computing: NERSC's Plan for 2006-2010." Report LBNL-57582, May 2005. Available as <http://www-library.lbl.gov/docs/LBNL/575/82/PDF/LBNL-57582.pdf>.
- [110] R. Nishtala, R. Vuduc, J. Demmel, K. Yelick, "Performance Modeling and Analysis of Cache Blocking in Sparse Matrix Vector Multiply." University of California, Berkeley, Computer Science Division Technical Report UCB/CSD-04-1335, June, 2004.
- [111] K. Yelick, D. Bonachea and C. Wallace, A Proposal for a UPC Memory Consistency Model, v1.0 (May 5, 2004), Lawrence Berkeley National Lab Tech Report LBNL-54983, 2004. Available from: <http://www-library.lbl.gov/docs/LBNL/549/83/PDF/LBNL-54983.pdf>
- [112] G. Griem, L. Oliker, J. Shalf, and K. Yelick, "Identifying Performance Bottlenecks on Modern Microarchitectures using an Adaptable Probe," Lawrence Berkeley National Laboratory Technical Report 54901, 2004. Available from <http://www-library.lbl.gov/docs/LBNL/549/01/PDF/LBNL-54901.pdf>
- [113] Performance Optimizations and Bounds for Sparse Symmetric Matrix-Multiple Vector Multiply. Benjamin C. Lee, Richard W. Vuduc, James W. Demmel, Katherine A. Yelick, Michael de Lorimier, Lijue Zhong. UCB/CSD-03-1297, November 2003.
- [114] Bell, C., D. Bonachea, Y. Cote, J. Duell, P. Hargrove, P. Husbands, C. Iancu, M. Welcome and K. Yelick (2003). An evaluation of current high-performance networks. Lawrence Berkeley National Laboratory Technical Report 52103, 2003. Available from: <http://www-library.lbl.gov/docs/LBNL/521/03/PDF/LBNL-52103.pdf>.
- [115] Brian G. Gaeke, Parry Husbands, Hyun Jin Kim, Xiaoye S. Li, Hyun Jin Moon, Leonid Oliker, Katherine A. Yelick, and Rupak Biswas, "Memory-intensive benchmarks: IRAM vs. cache-based machines." Lawrence Berkeley National Laboratory Technical Report LBNL-48979, 2002. Available from: <http://www-library.lbl.gov/docs/LBNL/489/79/PDF/LBNL-48979.pdf>.
- [116] W. Carlson, J. Draper, D. Culler, K. Yelick, E. Brooks, and K. Warren, "Introduction to UPC and Language Specification," CCS-TR-99-157, IDA Center for Computing Sciences, 1999.

- [117] A. Krishnamurthy, D. Culler, and K. Yelick, "Empirical Evaluation of Global Memory Support on the Cray-T3D and Cray-T3E," UCB//CSD-98-991, 1998.
- [118] L.V. Kale, J. Kohl, N. Chrisochoides, K. Yelick, "Concurrency-based Approaches to Parallel Programming," Scientific Computing. NASA, Report Number: CONF-9412112-1, 1996.
- [119] K. Yelick, C.-P. Wen, S. Chakrabarti, E. Deprit, J. Jones, A. Krishnamurthy, "Portable Parallel Irregular Applications," Workshop on Parallel Symbolic Languages and Systems, Beaune, France, October 1995. Lecture Notes in Computer Science.
- [120] S. Chakrabarti, E. Deprit, J. Jones, A. Krishnamurthy, E.-J. Im, C.-P. Wen, and K. Yelick, "Multipol: A Distributed Data Structure Library." UCB//CSD-95-879, July 1995.
- [121] K. Yelick, S. Chakrabarti, E. Deprit, J. Jones, A. Krishnamurthy, and C.-P. Wen, "Data Structures for Irregular Applications," DIMACS Workshop on Parallel Algorithms for Unstructured and Dynamic Problems, Piscataway, New Jersey, June 1993.
- [122] K. Yelick, "Using Abstraction in Explicitly Parallel Programs," MIT Laboratory for Computer Science, July 1991, TR-507. (Revised from PhD Thesis, December 1990.)
- [123] K. Yelick, A Generalized Approach to Equational Unificational, Master's Thesis, MIT Laboratory for Computer Science, August 1985, TR-344.

Professional Activities

Member of the DARPA Exascale Study Group: Technology Challenges in Achieving Exascale Systems, 2007-2008.

Program Co-Chair, Workshop on Automatic Tuning for Petascale Systems, Center for Scalable Application Development Systems (CScADS), 2007, 2008.

General Chair, ACM Conference on Principles and Practice of Parallel Programming (PPoPP), 2007

Program Committee, International Workshop on Multicore and Hybrid Systems for Numerically Intensive Computations, 2007.

Program Co-Chair, Workshop on programming models for HPCS ultra-scale applications, in conjunction with the International Conference on Supercomputing, 2005

Program Co-Chair, ACM Conference on Principles and Practice of Parallel Programming (PPoPP), 2005

Program Committee, Conference on Parallel Processing for Scientific Computing, 2004

Program Co-Chair, SIAM Conference on Parallel Processing for Scientific Computing, 1999

Program Committee, International Conference on Supercomputing (ICS), 2005

Program Committee, Irregular conference, 1997, 2000, 2001

Program Committee, Java Grande 2000

Invited Speakers Chair and Masterworks Co-Chair, SC2002

Program Committee, Supercomputing 1999 (SC99), 2000 (SC2000), 2003 (SC03) (Officially renamed to High Performance Computing and Networking, but still uses the SC Acronym and Supercomputing Proceedings.)

Program Committee, International Symposium on Computing in Object-oriented Parallel Environments (ISCOPE), 1999

Program Committee, Workshop on Languages, Compilers and Runtime Systems for Scalable Computers, 1998

Program Committee, Symposium on Parallel Algorithms and Architectures (SPAA), 1996, 1998, 2006

Program Committee, Programming Language Design and Implementation (PLDI), 1998, 2008

Program Committee, Principles of Programming Languages (POPL), 1998

Program Committee, International Parallel Processing Symposium and Symposium on Parallel and Distributed Computation (IPPS/SPDP), 1998

Program Committee, Principles and Practice of Parallel Programming (PPoPP), 1995, 2006

Program Committee, International Conference on Parallel Programming (ICPP), 1995

Program Committee, Workshop on Solving Irregular Problems on Distributed Memory Machines, 1995

Selection Committee, NSF CAREER program, 1994 and 1995

Program Committee, Object-Oriented Programming Systems, Languages, and Applications (OOPLSA), 1994 and 1995

Program Committee, Parallel Symbolic Computation, 1994

Organizational Committee of the Sigum User Interface Workshop on Parallel Programming Software, 1995.

Program Committee, Scalable High Performance Computing and Communication, 1994.

Treasurer, Principles and Practice of Parallel Programming, 1993

Registration Chair, International Symposium on Symbolic and Algebraic Computation, 1992
Secretary, SIAM Activity Group on Supercomputing, 1997-1999.

Selected Presentations and Invited Talks

“Programming Models for Parallel Machines”, UCB Bootcamp on Parallel Computing, August 25-36, Berkeley, CA.

“Multicore: Fallout from a Hardware Revolution,” Invited talk, South Dakota School of Mining and Technology, September 24, Rapid City, SD.

“Scheduling UPC Threads on GPUs and Multicore,” UPC Developers Workshop, September 22-23, Washington, DC.

“Programming Models for Manycore Processors,” Intel UPCRC Programming Languages Workshop, August 23, 2008, Santa Clara, CA.

“PERI, Tuning for Multicore,” SciDAC PI Meeting, Seattle, WA, July 14-17. (Filling in for scheduled speaker Sam Williams.)

“Programming Models: Opportunities and Challenges for Scalable Applications,” Next Generation Scalable Applications: When MPI Only is Not Enough. June 3-5, 2008.

“Programming Models for Manycore Systems,” Intel Corp., Santa Clara, CA, April 23, 2008. **Keynote.**

“Multicore Meets Exascale: The Catalyst for a Software Revolution,” 2008 Salishan Conference on High Speed Computing, Salishan, OR, April 21-22, 2008. **Keynote.**

“Programming Models for Petascale to Exascale,” IPDPS 2008, Miami, FL, April 15-16, 2008. **Keynote.**

“Multicore Meets Petascale: The Catalyst for a Software Revolution,” North Carolina State University, Raleigh, NC, Feb 10-12, 2008. Research Triangle Distinguished Lecture Series, Invited Talk.

“Programming Models for Petascale,” Princeton University, Princeton, NJ, February 25-26, 2008. Invited Talk.

“Programming Techniques to Harness Exaflops,” Frontiers of Extreme Scale Computing: From Nanoscale to Zettascale, Santa Cruz, California. October 21-25, 2007.

“Programming Model Issues in Petascale Computing,” Symposium on Turbulence & Dynamos at Petaspeed Boulder, Colorado, October 15-19, 2007.

“Productivity and Performance using Partitioned Global Address Space Languages,” Parallel Symbolic Computation (PASCO '07), London, Canada, July 27-28, 2007. Invited talk.

“Partitioned Global Address Space Languages for Multilevel Parallelism,” Center for Scalable Application Development Systems (CScADS) Workshop on Petascale Architectures. Snowbird, Utah, July 23-26, 2007. Invited talk.

“Automatic Performance Tuning Workshop,” Center for Scalable Application Development Systems (CScADS) Workshop on Automatic Performance Tuning. Snowbird, Utah, July 9-12, 2007. (Overview talk as program co-chair.)

“Partitioned Global Address Space Languages for Multilevel Parallelism,” Petascale Applications Symposium: Multilevel Parallelism and Locality-Aware Algorithms Pittsburgh Supercomputing Center, Pittsburgh, Pennsylvania, June 22-23, 2007. Invited talk.

“Tools and Libraries for Manycore Computing,” Manycore Computing Workshop, Seattle, Washington, June 20-21, 2007. Invited panel speaker.

“Parallel Languages: Past, Present and Future,” History of Programming Languages (HOPL-III), San Diego, California, June 9-10, 2007. Invited panel speaker.

“The Tenure Process,” CRA-W Career Mentoring Workshop, San Diego, California, June 9-10, 2007. Sponsored by the Computer Research Association's Committee on the Status of Women in Computing Research (CRA-W). Invited panel speaker.

“How to Write a Bad Proposal,” CRA-W Career Mentoring Workshop, San Diego, California, June 9-10, 2007. Sponsored by the Computer Research Association's Committee on the Status of Women in Computing Research (CRA-W). Invited panel speaker.

“The Berkeley View: Applications-Driven Research in Parallel Programming Models and Architectures,” Multicore-the New Face of Computing-Promises and Challenges, 8th IEEE/NATEA Annual Conference on New Frontiers in Computing Technology, June 2, 2007, Stanford University. **Keynote.**

“Compilation Techniques for PGAS Languages,” 5th Annual Workshop on Charm++ and its Applications, Parallel Programming Lab, University of Illinois at Urbana-Champaign April 18th-20th, 2007. **Keynote.**

“Architectural Trends and Programming Model Strategies for Large-Scale Machines,” MSRI Symposium on Climate Change, "From Global Models to Local Action." April 11-13, 2007. Invited talk.

“Overview of Titanium and the HPLS Program,” The Second Geoscience Application Requirements for Petascale Architectures, Feb 21-22, 2007, San Diego, California. Invited talk.

“Programming Models for Parallel Computing,” Interactive Parallel Computation in Support of Research in Algebra, Geometry and Number Theory, Berkeley, California, January 29-February 2, 2007. Invited talk.

“Compilation Techniques for Partitioned Global Address Space Languages,” The 19th International Workshop on Languages and Compilers for Parallel Computing, New Orleans, Louisiana, November 2-4, 2006. **Keynote.**

“Performance Advantages of Partitioned Global Address Space Languages,” EuroPVM/MPI '06, Bonn, Germany, September 17-20, 2006. Invited talk.

“Use of a high-level language in high performance biomechanics simulations.” Abstract appeared in the Journal of Biomechanics, “Abstracts of the 5th World Congress on Biomechanics,” July 29-August 4, 2006, Munich, Germany, p. S435.

“Optimizations for Partitioned Global Address Space Languages,” Thirteenth AURORA Plenary Meeting, Workshop on High Productivity Programming Language Systems, Strobl/Wolfgangsee, Austria, June 9-11, 2006. Invited talk.

“Using Meshes, Matrices, and Particles in Partitioned Global Address Space (PGAS) Languages,” Scientific Discovery through Advanced Computing (SciDAC), Denver, Colorado, June 25-29, 2006. Invited talk.

“Performance and Productivity Opportunities Using Global Address Space Programming Models,” PetaScale Computation for the Geosciences Workshop, San Diego Supercomputing Center, April 5, 2006.

“Using High Level Languages in Computational Frameworks,” Computational Frameworks (CompFrame) '05, Atlanta, Georgia, June 22-23, 2005. Invited talk.

“Finding a Research Topic,” CRA-W Graduate Cohort Program, San Francisco, California, February 25-26, 2005.

“Towards a Digital Human: Scalable Simulation of the Heart and Other Organs,” EECS Joint Colloquium

Distinguished Lecture Series, University of California at Berkeley, September 15, 2004. Invited talk.

“Towards a Digital Human: Simulation of the Heart and Other Organs,” Distinguished Lecture Series, University of California at Davis, April 2004. Invited talk.

“Programmability, Performance, and Portability of Global Address Space Languages,” High Performance Computing User Forum, Tucson, Arizona, September 21-22, 2004. Invited talk.

“Report on High-End Computing Research and Development in Japan,” Meeting of the Coalition for Academic Scientific Computation, July 14-15, 2004. Invited talk.

“Latency vs. Bandwidth: Which Matters More?” Workshop on Software for Processor-In-Memory Based Parallel Systems, at the Second Annual IEEE/ACM International Symposium on Code Generation and Optimization, San Jose, California, March 21, 2004. Invited talk.

“High Performance Programming in the Partitioned Global Address Space Model,” Short course co-taught with Tarek El-Ghazawi and Robert Numrich at the SIAM Conference on Parallel Processing for Scientific Computing, San Francisco, February 25-27, 2004.

“Titanium: A Java Dialect for High Performance Computing,” given as part of a tutorial on "UPC, Co-Array Fortran, and Titanium: Programming with the Partitioned Global Address Space Model." Supercomputing (SC03), November, 2003.

“Optimizing Java-Like Languages for Parallel and Distributed Environments,” Programming Language Design and Implementation, June 2001. Invited tutorial.

“Language and Compiler Support for Adaptive Mesh Refinement,” Caltech, Spring 2000. Invited talk.

“Exploiting On-Chip Memory Bandwidth in the VIRAM Compiler,” 2nd Workshop on Intelligent Memory Systems. In conjunction with Architectural Support for Programming Languages and Operating Systems, Boston Massachusetts, November 12, 2000.

“System Support for Data-Intensive Applications,” University of Washington, CRAW-Lucent Invited Lecture, Spring 2000.

“Titanium: A High Performance Java Dialect,” SIAM Conference on Parallel Processing for Scientific Computing, 1999.

“Compiling Explicitly Parallel Programs,” SIAM conference on Parallel Processing for Scientific Computing, 1997.

“Systems Support for Irregular Parallel Applications,” Irregular '96, Santa Barbara, California, August 19-21, 1996. Invited talk.

Co-authored Posters and Presentations

Eun-Jin Im, Cleve Ashcraft, Ismail Bustany, Katherine Yelick, “A Computationally Efficient Triple Matrix Product for a Class of Sparse Schur-Complement Matrices,” SIAM Conference on Parallel Processing for Scientific Computing. San Francisco, California, February 2004.

Dan Bonachea, Rajesh Nishtala, Paul Hargrove, Mike Welcome, Katherin Yelick, “Optimized Collectives for PGAS Languages with One-Sided Communication,” Supercomputing (SC06), November 2006

Dan Bonachea, Rajesh Nishtala, Paul Hargrove, Katherine Yelick, “Efficient Point-to-Point Synchronization in UPC,” 2nd Conf. on Partitioned Global Address Space Programming Models ([PGAS06](#)), October 2006

Dan O Bonachea, Christian Bell, Rajesh Nishtala, Kaushik Datta, Parry Husbands, Paul Hargrove, Katherine Yelick, "The Performance and Productivity Benefits of Global Address Space Languages," Supercomputing, November 2005.

Rajesh Nishtala, Richard Vuduc, James Demmel, and Katherine Yelick, "When Cache Blocking Sparse Matrix Multiply Works and Why." *PARA'04 Workshop on State-of-the-art in Scientific Computing*, Copenhagen, Denmark, June 2004.

E.-J. Im, I. Bustany, C. Ashcraft, J. Demmel, K. Yelick, "Toward automatic performance tuning of matrix triple products based on matrix structure." *PARA'04 Workshop on State-of-the-art in Scientific Computing*, Copenhagen, Denmark, June 2004. (Abstract only.) Full paper to appear in *Lecture Notes in Computer Science*.

Advising

Postdoctoral Researchers

Greg Balls

Eun-Jin Im

Ed Givelberg

PhD Students

Soumen Chakrabarti. PhD thesis title, "Efficient Resource Scheduling in Multiprocessors," June 1996. Master's report, "Computing Grobner Bases on a Distributed Memory Multiprocessor," December 1992.

Chih-Po Wen. PhD thesis title, "Portable Library Support for Irregular Applications," December 1995. Master's report, "Timing Simulation on Distributed Memory Multiprocessor," December 1992.

Arvind Krishnamurthy. PhD thesis title, "Compiler Analyses and System Support for Optimizing Shared Address Space Programs," December 1998. Master's report, "Compiling Explicitly Parallel Programs," May 1994.

Deborah Weisser. PhD thesis title, "Interacting Agents for Local Search," May 1999.

Eun-Jin Im, PhD thesis title, "Optimizing the Performance of Sparse Matrix-Vector Multiplication," May 2000.

Wei Chen. PhD thesis title, "Optimizing Partitioned Global Address Space Programs for Cluster Architectures," August 2007. Master's report, "Building a Source to Source UPC Translator," December 2004.

Jimmy Su. Master's report title, "Automatic Support for Irregular Computations in a High Level Languages," May 2005. PhD expected December 2009.

Dan Bonachea. Master's report title, "Bulk File I/O Extensions to Java," May 2000. PhD expected May 2009.

Rajesh Nishtala. Master's report title, "Architectural Probes for Measuring Communication Overlap Potential." May 2006. PhD expected December 2009.

Amir Kamil. Master's report title, "Analysis of Partitioned Global Address Space Programs," December 2006. PhD expected May 2011.

Kaushik Datta. Master's report title, "The NAS Parallel Benchmarks in Titanium," December 2005. PhD expected December 2009.

Shoaib Kamil. PhD expected May 2011.

Master's Students

Brian Kazian, Master expected August 2009.

Jason Duell, Master's report, "Pthreads or Processes: Which is Better for Implementing Global Address Space languages?" June 2007.

Christian Bell, "Design and Implementation of a Distributed Memory DMA Registration Strategy for Pinning – based High Performance Networks," May 2005.

Siu Man Yau, "Experiences in Using Titanium for Simulation of Immersed Boundary Biological Systems," May

2002.

Noah Treuhaft. "Enhancing Graduated Declustering for Better Performance Availability on Clusters," December 2000.

Chang-Sun Lin Master's report title, "The Performance Limitations of SPMD Programs on Clusters of Multiprocessors," May 2000.

Elaine Randi Thomas. Master's Report title, "An Architectural Performance Study of the Fast Fourier Transform on Vector IRAM," May 2000.

Ngeci Bowman. "Random Projection: A Data Compression Algorithm for EM" December 1999.

Jeff Jones. Master's report, "Parallelizing the Phylogeny Problem," December 1994.

Steve Steinberg. Master's report, "Parallelizing a Cell Simulation: Analysis, Abstraction, and Portability," December 1994.

Ruth Hinkins. Master's report, "Parallel Computation of Automatic Differentiation Applied to Magnetic Field Calculations," September 1994.

Undergraduate Research Students

Ankit Jain, 2005-2007

Wei Tu, 2004

Benjamin Lee, 2002-2004

Omair Kamil, 2004

Meling Ng, 2004

Siu Man Yau, 1999.

Kar Ming Tang, 1999.

Eric Reeber, 1999.

Glen Jeh, 1999.

Stanley H. Yue, 1999.

Andy Hung Ng, 1999

Sumeet Shendrikar, 1999

Anthony Lai, 1999.

Steve Benting, 1997-1998.

Karl Czajkowski, 1995-1996.

Daniel Yu, 1996.

Ronald Yong, 1996.

David Yan, 1996.

Jun Yang, 1995-1996.

Jenny Ng, 1994.

Boon-Yuen Ng, 1994.

Eric Liu, 1994.

Matthew Thorn, 1994.

Kevin Gong, 1992.

Dindo Siasoyco, 1992.