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Education

1985 B.S. and M.S. in Computer Science, Massachusetts Institute of Technology
1991 Ph.D. in Computer Science, Massachusetts Institute of Technology

Experience

University of California, Berkeley (1991-present)

Professor, Computer Science (2002-present)
Associate Professor, Computer Science (1996-2002)
Assistant Professor, Computer Science (1991-1996)

Lawrence Berkeley National Laboratory (1996-present)

Associate Laboratory Director for Computing Sciences, Lawrence Berkeley National Laboratory (2010-present)
National Energy Research Scientific Computing (NERSC) Division Director (2008-present)
Future Technologies Group Lead (2005-2007)
Faculty Research Scientist (1996-2005)

ETH, Zurich, Switzerland (Summer, 1996)

Visiting Researcher

Massachusetts Institute of Technology (Fall, 1996)

Visiting Associate Professor

Clark University (Spring, 1985)

Visiting Instructor

Awards and Honors

- Best Paper Award, International Parallel and Distributed Processing Symposium, 2008.
- Okawa Foundation Research Grant 2005.
- Best Paper Award, International Conference on Parallel Processing, 2004.
- Best Student Paper Award, ICS 2002: Workshop on Performance Optimization via High-Level Languages and Libraries.
- Computer Science Division Diane S. McEntyre Award for Excellence in Teaching, U.C. Berkeley, 2001.
- ARO Young Investigator Award, 1996.
- George M. Sprows Award for Best PhD Dissertation, EECS Department at MIT, 1991.
- Teaching award with promotion to Instructor "G" from EECS Department at MIT, 1987.
- Best Student Paper Award, Rewriting Techniques and Applications, 1985.

National and International Technical Leadership

- Computer Science and Telecommunications Board (CSTB), an advisory board of the National Academies, 2011-present.
- Massachusetts Institute of Technology, Electrical Engineering and Computer Sciences Visiting Committee, 2011-2016.
- National Academies panel on "Sustaining the Growth in Computing Performance", 2007-2011
- Department of Energy, Exascale ("E7") Executive Committee, 2011.

- U.S. Congressional Briefing on “Supercomputing for Science and Competitiveness,” 2011.
- Blue Ribbon Panel for Computing Science (BRPCS) in Qatar, advising Qatar Foundation, 2011.
- DARPA High Productivity Computing Systems program review team, 2010-2011.
- Defense Research and Engineering (DDRE) Computer Science research planning workshop, May 2011.
- NSF Task Force on Critical Cyberinfrastructure for Advancing Science and Engineering, 2009.
- DARPA Exascale Study Group: Technology Challenges in Achieving Exascale Systems, 2007-2008.
- WTEC Committee on the Assessment of High-End Computing Research and Development in Japan, report sponsored by NSF and DOE, 2004.

Publications

Books and Book Chapters

- [1] “The Future of Computing Performance: Game Over or Next Level?” Samuel H. Fuller and Lynette I. Millett, Editors; Committee on Sustaining Growth in Computing Performance (Samuel H. Fuller, Luiz Andrew Barroso, Robert P. Colwell, William J. Dally, Dan Dobberpuhl, Mark D. Hill, Pradeep Dubey, Mark D. Hill, Mark Horowitz, David Kirk, Monica Lam, Kathryn S. McKinley, Charles Moore, Katherine Yelick); National Research Council, 2011.
- [2] “Auto-tuning Stencil Computations on Diverse Multicore Architectures”, K. Datta, S. Williams, V. Volkov, J. Carter, L. Oliker, J. Shalf, K. Yelick; chapter in Scientific Computing with Multicore and Accelerators; Editors Jack Dongarra, David A. Bader, Jakub Kurzak, CRC Press 2010.
- [3] "Auto-Tuning Memory-Intensive Kernels for Multicore", S. Williams, K. Datta, L. Oliker, J. Carter, J. Shalf, Y. Yelick, chapter in Performance Tuning of Scientific Applications, Editors D. H. Bailey, R. F. Lucas, S. W. Williams, CRC Press, November 2010.
- [4] “ExaScale Computing Study: Technology Challenges in Achieving Exascale Systems,”_Peter Kogge (Editor & Study Lead), Keren Bergman, Shekhar Borkar, Dan Campbell, William Carlson, William Dally, Monty Denneau, Paul Franzon, William Harrod, Kerry Hill, Jon Hiller, Sherman Karp, Stephen Keckler, Dean Klein, Robert Lucas, Mark Richards, Al Scarpelli, Steven Scott, Allan Snavely, Thomas Sterling, R. Stanley Williams, Katherine Yelick, September 28, 2008. Published by the Air Force Research Laboratory. Available from http://users.ece.gatech.edu/~mrichard/ExascaleComputingStudyReports/ECS_reports.htm.
- [5] “Assessment of High-End Computing Research and Development in Japan,” Al Trivelpiece, Rupak Biswas, Jack Dongarra, Peter Paul, Katherine Yelick, World Technology Evaluation Center, Inc., 2004. Available from <http://www.wtec.org/reports.htm>.
- [6] “UPC: Distributed Shared-Memory Programming,” Tarek El-Ghazawi, William Carlson, Thomas Sterling, and Katherine Yelick, Wiley-Interscience, May 2005.

Refereed Journal and Conference Papers

- [7] Filip Blagojevic', Paul Hargrove, Costin Iancu, Katherine Yelick. “Hybrid PGAS Runtime Support for Multicore Nodes,” Partitioned Global Address Space (PGAS) conference, New York, NY, October 12, 2010.
- [8] S. Williams, J. Carter, L. Oliker, J. Shalf, K. Yelick, "*Optimization of a Lattice Boltzmann Computation on State-of-the-Art Multicore Platforms*", Journal of Parallel and Distributed Computing (JPDC), 2009. doi: 10.1016/j.jpdc.2009.04.002.
- [9] K. Datta, S. Williams, V. Volkov, J. Carter, L. Oliker, J. Shalf, K. Yelick "*Auto-tuning the 27-point Stencil for Multicore*", 4th International Workshop on Automatic Performance Tuning (iWAPT), 2009.
- [10] Kamesh Madduri, Samuel Williams, Stephane Ethier, Leonid Oliker, John Shalf, Erich Strohmaier, Katherine A. Yelick, "Memory-Efficient Optimization of Gyrokinetic Particle-to-Grid Interpolation for Multicore Processors," SC09: International Conference for High-Performance Computing, Networking, Storage, and Analysis, Nov, 2009. Proceedings of the ACM/IEEE Conference on Supercomputing (SC09), Portland, OR, November 2009.
- [11] Marghoob Mohiyuddin, Mark Hoemmen, James Demmel, Katherine Yelick, “Minimizing Communication in Sparse Matrix Solvers,” Proceedings of the ACM/IEEE Conference on Supercomputing (SC09), Portland, OR, November 2009.
- [12] Krste Asanovic, Rastislav Bodik, James Demmel, Tony Keaveny, Kurt Keutzer, John Kubiawicz, Nelson Morgan, David Patterson, Koushik Sen, John Wawrzynek, David Wessel, and Katherine Yelick, “A View of the Parallel Computing Landscape,” Communications of the ACM, November 2009.

- [13] Amir Kamil and Katherine Yelick, "Enforcing Textual Alignment of Collectives Using Dynamic Checks," 22nd International Workshop on Languages and Compilers for Parallel Computing (LCPC), October 2009. Appeared in Springer-Verlag Lecture Notes in Computer Science, 2010, Volume 5898/2010, 368-382, DOI: 10.1007/978-3-642-13374-9_25.
- [14] Bryan Catanzaro, Shoaib Kamil, Yunsup Lee, Krste Asanovic, James Demmel, Kurt Keutzer, John Shalf (LBL), Kathy Yelick, Armando Fox. SEJITS: Getting Productivity And Performance With Selective, Just-In-Time Specialization. Proc. 1st Workshop on Programming Models for Emerging Architectures (PMEA'09), Raleigh, NC, Sept. 2009.
- [15] Dan Bonachea, Paul Hargrove, Michael Welcome, Katherine Yelick, "Porting GASNet to Portals: Partitioned Global Address Space (PGAS) Language Support for the Cray XT," Proceedings of the Cray User Group (CUG), Atlanta, GA, May 2009.
- [16] Samuel Williams, Jonathan Carter, Leonid Oliker, John Shalf, and Katherine Yelick, "Hierarchical Auto-Tuning of a Hybrid Lattice-Boltzmann Computation on the XT4 and XT5," Proceedings of the Cray User Group (CUG), Atlanta, GA, May 2009.
- [17] Rajesh Nishtala, Paul Hargrove, Dan Bonachea, Katherine Yelick, "Scaling Communication-Intensive Applications on BlueGene/P Using One-Sided Communication and Overlap," 23rd International Parallel & Distributed Processing Symposium (IPDPS), Rome, Italy, May 2009.
- [18] Rajesh Nishtala, Katherine Yelick, "Optimizing Collective Communication on Multicores," HotPar 2009, Berkeley, CA, March 2009.
- [19] Joseph Gebis, Leonid Oliker, John Shalf, Samuel Williams, Katherine A. Yelick: Improving Memory Subsystem Performance Using ViVA: Virtual Vector Architecture. Architecture of Computing Systems - ACS 2009, 22nd International Conference, Delft, The Netherlands, March 10-13, 2009. Lecture Notes in Computer Science 5455 Springer 2009, ISBN 978-3-642-00453-7146-158.
- [20] Sam Williams, Kaushik Datta, Jonathan Carter, Leonid Oliker, John Shalf, Katherine Yelick, David Bailey, PERI - Auto-tuning Memory Intensive Kernels for Multicore, SciDAC: Scientific Discovery Through Advanced Computing, Seattle Washington, July, 2008. Journal of Physics: Conference Series. LBNL # pending.
- [21] Kaushik Datta, Shoaib Kamil, Sam Williams, Leonid Oliker, John Shalf, Katherine Yelick, "Optimization and Performance Modeling of Stencil Computations on Modern Microprocessors", SIAM Review, vol. 51, issue 1, 2009, pp. 129-159. (Cover story.) Also appeared as LBNL Technical Report number LBNL-63192.
- [22] Kaushik Datta, Mark Murphy, Vasily Volkov, Samuel Williams, Jonathan Carter, Leonid Oliker, David Patterson, John Shalf, and Katherine Yelick, "Stencil Computation Optimization and Autotuning on State-of-the-Art Multicore Architectures," Proceedings of the ACM/IEEE Conference on Supercomputing (SC08), November 2008. LBNL # Pending.
- [23] Samuel Williams, David A. Patterson, Leonid Oliker, John Shalf, Katherine Yelick, "The Roofline Model: A pedagogical tool for auto-tuning kernels on multicore architectures", HOT Chips, A Symposium on High Performance Chips, Stanford, CA, Aug 2008. (Abstract.)
- [24] Costin Iancu, Wei Chen, Katherine A. Yelick: Performance portable optimizations for loops containing communication operations. International Conference on Supercomputing (ICS), Island of Kos, Greece, June 7-12, 2008, pages 266-276.
- [25] J. Demmel, M. Hoemmen, M. Mohiyuddin, K. Yelick, "Avoiding Communication in Sparse Matrix Computations," IEEE Intern. Parallel and Distributed Processing Symposium (IPDPS'08), April 2008.
- [26] Samuel Williams, Jonathan Carter, Leonid Oliker, John Shalf, Katherine Yelick, "Lattice Boltzmann Simulation Optimization on Leading Multicore Platforms," IEEE International Parallel and Distributed Processing Symposium (IPDPS'08), April 2008. **Best Paper Award**, Applications Track.
- [27] Jimmy Su and Katherine Yelick, "Automatic Communication Performance Debugging in PGAS Languages" 20th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Urbana, Illinois, October 2007. Lecture Notes in Computer Science 5234 Springer 2008, ISBN 978-3-540-85260-5.
- [28] Parry Husbands and Katherine Yelick, "Multithreading and One-Sided Communication in Parallel LU Factorization." Proceedings of Supercomputing (SC07), Reno, NV, November, 2007.
- [29] Tong Wen, Jimmy Su, Phillip Colella, Katherine Yelick and Noel Keen, "An Adaptive Mesh Refinement Benchmark for Modern Parallel Programming Languages." Proceedings of Supercomputing (SC07), Reno, NV, November 2007.
- [30] Sam Williams, Leonid Oliker, Richard Vuduc, John Shalf, Katherine Yelick, James Demmel, "Optimization of Sparse Matrix-Vector Multiplication on Emerging Multicore Platforms." Proceedings of Supercomputing (SC07), November 2007.

- [31] Amir Kamil and Katherine Yelick, "Hierarchical Pointer Analysis for Distributed Programs," Static Analysis Symposium (SAS), Kongens Lyngby, Denmark, August 22-24, 2007.
- [32] Katherine Yelick, Paul Hilfinger, Susan Graham, Dan Bonachea, Jimmy Su, Amir Kamil, Kaushik Datta, Phillip Colella, and Tong Wen, "Parallel Languages and Compilers: Perspective from the Titanium Experience." *Journal of High Performance Computing Applications*, August 2007, vol. 21, pp. 266-290.
- [33] K. Yelick, D. Bonachea, W.-Y. Chen, P. Colella, K. Datta, J. Duell, S. Graham, P. Hargrove, P. Hilfinger, P. Husbands, C. Iancu, A. Kamil, R. Nishtala, J. Su, M. Welcome, T. Wen, "Productivity and Performance Using Partitioned Global Address Space Languages," *Proceedings of Parallel Symbolic Computation (PASCO)*, London, Ontario, July 27-28, 2007.
- [34] Alfredo Buttari, Jack Dongarra, Parry Husbands, Jakob Kurzak and Katherine Yelick, "Multithreading for synchronization tolerance in matrix factorization," *Proceedings of the SciDAC 2007 Conference*, Boston, Massachusetts, July 24-28, 2007. Published in the *Journal of Physics: Conference Series*. Volume 78, 2007, June, 2007.
- [35] Wei Chen, Dan Bonachea, Costin Iancu, and Katherine Yelick, "Automatic Nonblocking Communication for Partitioned Global Address Space Programs," *Proceedings of the International Conference on Supercomputing (ICS)*, Seattle, Washington, June 16-17, 2007.
- [36] Shivali Agarwal, Rajkishore Barik, Dan Bonachea, Vivek Sarkar, Rudrapatna Shyamasundar, Katherine Yelick, "Deadlock-Free Scheduling of X10 Computations with Bounded Resources," *Symposium on Parallel Algorithms and Architecture (SPAA)*, San Diego California, June 9-11, 2007.
- [37] Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands, and Katherine Yelick, "Scientific Computing Kernels on the Cell Processor," *International Journal of Parallel Programming (IJPP)*, DOI 10.1007/s10766-007-0034-5, April 2007.
- [38] Ewing Lusk and Katherine Yelick, "Languages for High-Productivity Computing: The DARPA HPCS Language Project," *Parallel Processing Letters*, Vol. 17, No. 1, March 2007, pp. 89-102.
- [39] Rajesh Nishtala, Richard Vuduc, James Demmel, and Katherine Yelick, "When Cache Blocking Sparse Matrix Multiply Works and Why." *Applicable Algebra in Engineering, Communication and Computing*, March 2007.
- [40] Hormozd Gahvari, Mark Hoemmen, James Demmel, Katherine Yelick, "Benchmarking Sparse Matrix-Vector Multiply in Five Minutes," *SPEC Benchmark Workshop 2007*, Austin, TX, January 2007.
- [41] Hongzhang Shan, Erich Strohmaier, Ji Qiang, David H. Bailey, and Kathy Yelick, "Performance Modeling and Optimization of a High Energy Colliding Beam Simulation Code," *Proceedings of SC2006*, Nov 2006. Also appeared as Lawrence Berkeley National Laboratory Technical Report, LBNL-60180.
- [42] Shoaib Kamil, Kaushik Datta, Sam Williams, Leonid Oliker, John Shalf, Katherine Yelick, "Implicit and Explicit Optimizations for Stencil Computations," *ACM Workshop on Memory Systems Performance and Correctness*, San Jose, California, October 22, 2006.
- [43] Katherine Yelick, "Performance Advantages of Partitioned Global Address Space Languages," *Recent Advances in Parallel Virtual Machine and Message Passing Interface*, Lecture Notes in Computer Science, Springer Berlin / Heidelberg, Volume 4192/2006, September 21, 2006. (Short abstract only.)
- [44] Edward Givelberg, Katherine Yelick, "Distributed Immersed Boundary Simulations in Titanium." *SIAM Journal on Scientific Computing*, Volume 28 Issue 4, Pages 1361-1378, August 7, 2006.
- [45] Sam Williams, John Shalf, Leonid Oliker, Parry Husbands, Shoaib Kamil, Katherine Yelick, "The Potential of the Cell Processor for Scientific Computation," *ACM International Conference on Computing Frontiers*, Ischia, Italy, May 2-5, 2006.
- [46] Christian Bell, Dan Bonachea, Rajesh Nishtala, and Katherine Yelick, "Optimizing Bandwidth Limited Problems Using One-Sided Communication and Overlap," *20th International Parallel & Distributed Processing Symposium (IPDPS)*, Rhodes Island, Greece, April 25-29, 2006. Also available as Lawrence Berkeley National Lab Tech Report LBNL-59207.
- [47] Eun-Jin Im, Ismail Bustany, Cleve Ashcraft, James W. Demmel, and Katherine A. Yelick "Performance Tuning of Matrix Triple Products Based on Matrix Structures," *Springer Lecture Notes in Computer Science, Applied Parallel Computing: State of the Art in Scientific Computing: Revised Selected Papers from the 7th International Workshop, PARA 2004 Lyngby, Denmark, June 20-23, 2004*; Springer-Verlag New York Inc, March 15, 2006, pp. 740-746.
- [48] Amir Kamil, Jimmy Su, and Katherine Yelick, "Making Sequential Consistency Practical in Titanium." *Supercomputing 2005 (SC05)*, Seattle, Washington, November 2005.

- [49] Amir Kamil and Katherine Yelick, "Concurrency Analysis for Parallel Programs with Textually Aligned Barriers." 18th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Hawthorne, New York, October 2005.
- [50] Kaushik Datta, Dan Bonachea and Katherine Yelick. "Titanium Performance and Potential: an NPB Experimental Study." 18th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Hawthorne, New York, October 2005.
- [51] Wei-Yu Chen, Costin Iancu, and Katherine Yelick, "Communication Optimizations for Fine-grained UPC Applications," 14th International Conferences on Parallel Architectures and Compilation Techniques (PACT '05), St. Louis, MO, Sept. 17-21, 2005.
- [52] J. Demmel, K. Yelick, and R. Vuduc. "OSKI: An Automatically Tuned Library of Sparse Matrix Kernels." Proceedings of SciDAC Conference 2005, Scientific Discovery through Advanced Computing, 26-30 June 2005, San Francisco, CA, USA. Published in the Journal of Physics: Conference Series, Volume 16, 2005.
- [53] S. Kamil, P. Husbands, J. Shalf, L. Oliker, K. Yelick, "Impact of Modern Memory Subsystems on Cache Optimizations for Stencil Computations," 3rd Annual ACM SIGPLAN Workshop on Memory Systems Performance, June 2005.
- [54] J. Demmel, J. Dongarra, V. Eijkhout, E. Fuentes, A. Petitet, R. Vuduc, R. C. Whaley, K. Yelick, "Self-Adapting Linear Algebra Algorithms and Software." Proceedings of the IEEE, Special Issue on Program Generation, Optimization, and Adaptation, vol. 93, no. 2, February 2005.
- [55] J. Su and K. Yelick, "Automatic Support for Irregular Computations in a High-Level Language," 19th International Parallel and Distributed Processing Symposium (IPDPS), Denver, Colorado, April 2005.
- [56] M. Narayanan and K. Yelick, "Generating permutation instructions from a high level description." 6th Workshop on Media and Streaming Processors, Portland, Oregon, December 5, 2006.
- [57] B. Lee, R. Vuduc, J. Demmel, K. Yelick, "Performance Models for Evaluation and Automatic Tuning of Symmetric Sparse Matrix-Vector Multiply," *International Conference on Parallel Processing*, Montreal, Quebec, Canada, August 2004. Winner, **Best Paper Award**.
- [58] C. Bell, W. Chen, D. Bonachea, and K. Yelick, "Evaluating Support for Global Address Space Languages on the Cray X1." International Conference on Supercomputing (ICS'04), Saint-Malo, France, June 2004.
- [59] J. Su and K. Yelick, "Array Prefetching for Irregular Array Accesses in Titanium" 6th International Workshop on Java™ for Parallel and Distributed Computing, Santa Fe, New Mexico, April 2004.
- [60] G. Griem, L. Oliker, J. Shalf, and K. Yelick, "Identifying Performance Bottlenecks on Modern Microarchitectures using an Adaptable Probe," Workshop on Performance Modeling, Evaluation, and Optimization of Parallel and Distributed Systems, Santa Fe, New Mexico, April 2004. Also appeared as LBNL Technical Report 54901.
- [61] E.-J. Im, K. Yelick, and R. Vuduc, "SPARSITY: An Optimization Framework for Sparse Matrix Kernels." International Journal of High Performance Computing Applications, 18 (1), pp. 135-158, 2004.
- [62] Wei-Yu Chen, Arvind Krishnamurthy, Katherine Yelick, "Polynomial-time Algorithms for Enforcing Sequential Consistency in SPMD Programs with Arrays," 16th International Workshop on Languages and Compilers for Parallel Computing (LCPC), College Station, Texas, October 2003.
- [63] W. Chen, D. Bonachea, J. Duell, P. Husbands, C. Iancu, K. Yelick, "A Performance Analysis of the Berkeley UPC Compiler," 17th Annual International Conference on Supercomputing (ICS), San Francisco, California, June 2003.
- [64] Richard Vuduc, Attila Gyulassy, James W. Demmel, Katherine A. Yelick, "Memory Hierarchy Optimizations and Performance Bounds for Sparse $A^T A * x$," ICCS 2003: Workshop on Parallel Linear Algebra. Melbourne, Australia, June 2003.
- [65] C. Bell, D. Bonachea, Y. Cote, J. Duell, P. Hargrove, P. Husbands, C. Iancu, M. Welcome, K. Yelick, "An Evaluation of Current High Performance Networks," International Parallel and Distributed Processing Symposium, Nice, France, April 22-26, 2003.
- [66] Ben Liblit, Alex Aiken and Katherine Yelick, "Type Systems for Distributed Data Sharing," 10th International Static Analysis Symposium, June 11-13, 2003, San Diego, California. Also appeared as: Static Analysis, Lecture Notes in Computer Science, 2003, Volume 2694/2003, 1075, DOI: 10.1007/3-540-44898-5_15.
- [67] R. Vuduc, J. Demmel, K. Yelick, S. Kamil, R. Nishtala, B. Lee. "Performance Optimizations and Bounds for Sparse Matrix-Vector Multiply." Proceedings of the IEEE/ACM Conference on High Performance Computing and Communications ("Supercomputing"), SC02, Baltimore, November, 2002.
- [68] R. Vuduc, S. Kamil, J. Hsu, R. Nishtala, J. Demmel, K. Yelick. "Automatic Performance Tuning and Analysis of Sparse Triangular Solve." ICS 2002: Workshop on Performance Optimization via High-Level Languages and Libraries, New York, June 22, 2002. **Best Student Paper and Best Student Presentation..**

- [69] Brian R. Gaeke, Parry Husbands, Xiaoye S. Li, Leonid Oliker, Katherine A. Yelick, and Rupak Biswas. "Memory-Intensive Benchmarks: IRAM vs. Cache-Based Machines," Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS). Ft. Lauderdale, FL. April, 2002.
- [70] D. Oppenheimer, A. Brown, J. Beck, D. Hettena, J. Kuroda, N. Treuhaft, D.A. Patterson, and K. Yelick, "ROC-1: Hardware Support for Recovery-Oriented Computing." IEEE Transactions on Computers, vol. 51, no. 2, pp. 100-107, Feb. 2002. Special Issue on Embedded Fault-Tolerant Computer Systems.
- [71] Christoforos Kozyrakis, David Judd, Joeseeph Gebis, Samuel Williams, David Patterson, Katherine Yelick, "Hardware/compiler Codevelopment for an Embedded Media Processor," *Proceedings of the IEEE*, vol. 89, no. 11, pages 1694-1709, November 2001.
- [72] E.-J. Im and K. Yelick, "Optimizing Sparse Matrix Computations for Register Reuse in Sparsity," Proceedings of the International Conference on Computational Science, San Francisco, May 2001.
- [73] E.-J. Im and K. Yelick, "Optimization of Sparse Matrix Kernels for Data Mining," Proceedings of Text Mine Workshop '01, Chicago, April 7, 2001.
- [74] D. Judd, K. Yelick, C. Kozyrakis, D. Martin, and D. Patterson, "Exploiting On-Chip Memory Bandwidth in the VIRAM Compiler," Second Workshop on Intelligent Memory Systems, Cambridge, November 2000.
- [75] T. Nguyen, A. Zakhor and K. Yelick, "Performance Analysis of an H.263 Video Encoder on VIRAM," International Conference on Image Processing (ICIP), Vancouver, B.C., Canada, September 2000.
- [76] R. H. Arpaci-Dusseau, E. Anderson, N. Treuhaft, D. E. Culler, J. M. Hellerstein, D. A. Patterson, and K. A. Yelick, "Cluster I/O with River: Making the Fast Case Common, Workshop on I/O in Parallel and Distributed Systems," Atlanta, GA, May 1999.
- [77] Randi Elaine Thomas and Katherine Yelick, "Efficient FFTs on VIRAM", Proceeding of the 1st Workshop on Media Processors and DSPs, in Conjunction with the 32nd Annual International Symposium on Microarchitecture, Haifa, Israel, November 15, 1999.
- [78] E. Im and K. A. Yelick, "Optimizing Sparse Matrix Vector Multiplication on SMPs," SIAM Conf. Parallel Processing for Scientific Computing, San Antonio, TX, March 1999.
- [79] E. Im and K. A. Yelick, "Model-based Memory Hierarchy Optimizations for Sparse Matrices," Workshop on Profile and Feedback-Directed Compilation, Paris, France, October 1998.
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- [81] S. Chakrabarti, J. Demmel, and K. Yelick. "Models and Scheduling Algorithms for Mixed Data and Task Parallel Programs." *Journal of Parallel and Distributed Computing*, Vol. 47, pp. 168--184. December 1997.
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- [88] Krishnamurthy and K. Yelick, "Analyses and Optimizations for Shared Address Space Programs." *Journal of Parallel and Distributed Computation*, vol.38, (no.2), Academic Press, 1 Nov. 1996. pp.130--44.
- [89] S. Steinberg, J. Yang and K. Yelick, "Performance Modeling and Composition: A Case Study in Cell Simulation." International Parallel Processing Symposium, April 1996.

- [90] J. Jones and K. Yelick, "Parallelizing the Phylogeny Problem" Supercomputing '95, San Diego, California, December 1995.
- [91] C.-P. Wen and K. Yelick, "Portable Runtime Support for Asynchronous Simulation." Proceedings of the International Conference on Parallel Processing, Oconomowoc, Wisconsin, August 1995.
- [92] S. Chakrabarti, J. Demmel, and K. Yelick, "Modeling the Benefits of Mixed Data and Task Parallelism," Proceedings of the Symposium on Parallel Algorithms and Architectures, Santa Barbara, California, July 1995.
- [93] Krishnamurthy and K. Yelick, "Optimizing Parallel Programs with Explicit Synchronization." Proceedings of the ACM Conference on Programming Language Design and Implementation (PLDI), San Diego, California, June 1995.
- [94] R. Arpaci, D. Culler, A. Krishnamurthy, S. Steinberg, and K. Yelick, "Empirical Evaluation of the CRAY-T3D: A Compiler Perspective," International Symposium on Computer Architecture, Santa Margherita Ligure, Italy, June 1995.
- [95] S.-T. Cheng, R. Brayton, G. York, K. Yelick, A. Saldana, "Compiling Verilog into Finite State Machines," International Verilog Conference, 1995.
- [96] S. Chakrabarti and K. Yelick, "Distributed Data Structures and Algorithms for Grobner Basis Computation," Lisp and Symbolic Computation, Volume 7, 1994, Pages 147--172.
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Non-refereed Reports

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- [144] K. Yelick, A Generalized Approach to Equational Unification, Master's Thesis, MIT Laboratory for Computer Science, August 1985, TR-344.

Professional Activities

Program Chair and Co-Chair

- Program Co-Chair, International Parallel and Distributed Processing Symposium (IPDPS) 2012
- Program Co-Chair, Workshop on Automatic Tuning for Petascale Systems, Center for Scalable Application Development Systems (CScADS), 2007, 2008.
- General Chair, ACM Conference on Principles and Practice of Parallel Programming (PPoPP), 2007
- Program Co-Chair, Workshop on programming models for HPCS ultra-scale applications, in conjunction with the International Conference on Supercomputing, 2005
- Program Co-Chair, ACM Conference on Principles and Practice of Parallel Programming (PPoPP), 2005
- Program Co-Chair, SIAM Conference on Parallel Processing for Scientific Computing, 1999

Review Committees

- Lehman Review Committee, Argonne Leadership Computing Center, July 2009.
- Lehman Review Committee, Oak Ridge Leadership Computing Center, February 2008.
- Lehman Review Committee, Oak Ridge Leadership Computing Center, December 2010.

Editorial Boards and Program Committees

- Program Co-Chair, International Parallel and Distributed Processing Symposium (IPDPS), Shanghai, China, May 2012.
- Program Committee, SC09 Workshop, “Curricula for Concurrency and Parallelism,” IEEE/ACM Conference on Supercomputing (SC09), Portland, Oregon, November 2009.
- Partitioned Global Address Space (PGAS) Workshop, Program Committee, 2009.
- SciDAC PI Meeting, Program Committee, 2009.
- SciDAC Review (editorial) Board Member, 2008, 2009.
- Program Committee, International Workshop on Multicore and Hybrid Systems for Numerically Intensive Computations, 2007.
- Program Committee, Conference on Parallel Processing for Scientific Computing, 2004
- Program Committee, International Conference on Supercomputing (ICS), 2005
- Program Committee, Irregular conference, 1997, 2000, 2001
- Program Committee, Java Grande 2000
- Program Committee, Supercomputing 1999 (SC99), 2000 (SC2000), 2003 (SC03) (Officially renamed to High Performance Computing and Networking, but still uses the SC Acronym and Supercomputing Proceedings.)
- Invited Speakers Chair and Masterworks Co-Chair, SC2002 (“Supercomputing”)
- Program Committee, International Symposium on Computing in Object-oriented Parallel Environments (ISCOPE), 1999
- Program Committee, Workshop on Languages, Compilers and Runtime Systems for Scalable Computers, 1998
- Program Committee, Symposium on Parallel Algorithms and Architectures (SPAA), 1996, 1998, 2006
- Program Committee, Programming Language Design and Implementation (PLDI), 1998, 2008
- Program Committee, Principles of Programming Languages (POPL), 1998
- Program Committee, International Parallel Processing Symposium and Symposium on Parallel and Distributed Computation (IPPS/SPDP), 1998
- Program Committee, Principles and Practice of Parallel Programming (PPoPP), 1995, 2006
- Program Committee, International Conference on Parallel Programming (ICPP), 1995
- Program Committee, Workshop on Solving Irregular Problems on Distributed Memory Machines, 1995
- Selection Committee, NSF CAREER program, 1994 and 1995
- Program Committee, Object-Oriented Programming Systems, Languages, and Applications (OOPLSA), 1994 and 1995
- Program Committee, Parallel Symbolic Computation, 1994
- Organizational Committee of the Signum User Interface Workshop on Parallel Programming Software, 1995.
- Program Committee, Scalable High Performance Computing and Communication, 1994.
- Treasurer, Principles and Practice of Parallel Programming, 1993
- Registration Chair, International Symposium on Symbolic and Algebraic Computation, 1992
- Secretary, SIAM Activity Group on Supercomputing, 1997-1999.

Software Releases

Berkeley UPC Compiler: The Berkeley UPC compiler is an Open Source translator for the UPC language, which runs on most supercomputers (in particular Cray XT, IBM BlueGene, IBM Power machines), Linux clusters with Infiniband, Myrinet, or Ethernet networks, shared memory multiprocessors, as well as personal computers. The compiler and runtime package is released annually and is used by the research community, in parallel programming classes, and in a production setting by government agencies. Multiple companies have used the Berkeley compiler when bidding on large procurements that require a UPC compiler. UPC as a language is popular within the defense community and there are several commercial and open implementations. The translator has also been used as a research platform for studying compiler and runtime optimizations for explicitly parallel code.

GASNet Communication Layer: GASNet is the Global Address Space Networking layer that was originally developed for the Berkeley Titanium and UPC runtime systems. It provides fast one-sided communication (put/get) as well as active messages, locks, and collective communication. GASNet has become a pseudo standard for one-sided communication, and is used now in the commercial Cray UPC and Co-Array Fortran compilers for the XT platforms, by the Cray Chapel project, by the Intrepid gcc-based implementation, and by several research efforts in parallel libraries. It has also influenced the development MPI's one-sided communication—demonstrating some of the limitations of that original one-sided specification in MPI—and the group is often consulted on what type of hardware support high speed interconnects need to support these languages.

Titanium Compiler and Runtime: The Titanium language is a Java dialect with extensions for parallel scientific programming. Like UPC, it is an example of a class of languages now known as Partitioned Global Address Space (PGAS) language. The Titanium compiler had several public releases, and was used by groups internationally for experimenting with parallel languages. (Titanium is a joint project with Susan Graham, Paul Hilfinger, and Alex Aiken, along with several students.)

Sparsity Library: Sparsity was the first library that used autotuning for sparse matrices. The optimizations include filling in zeros to create uniform register blocks, cache blocking and serial optimizations to improve scheduling by the backend C compiler. Sparsity uses offline search over dense matrix in various sparse formats to instantiate a performance model that is used for online selection of matrix format an associated algorithm.

OSKI Library: The OSKI library was done jointly with Jim Demmel and our student, Rich Vuduc (now on the faculty at Georgia Tech). OSKI builds on the ideas on Sparsity, but is a complete redesign that contains an extensible code generation framework, new performance models, optimization across multiple functional calls, and support for preserving history information across library uses.

Selected Presentations and Invited Talks

“To Virtualize or Not to Virtualize,” ASCR Workshop on Exascale Programming Challenges, Marina del Rey, California, August 2011.

“Exascale Opportunities and Challenges,” Society of Exploration Geophysics Workshop on High Performance Computing in the Geosciences, Berkeley, California, July 2011. **Invited Talk.**

“Exascale Opportunities and Challenges,” The 20th International ACM Symposium on High-Performance Parallel and Distributed Computing, San Jose, California, June 8-11, 2011. **Keynote.**

“Autotuning in the Exascale Era,” International Workshop on Adaptive Self-Tuning Computing Systems for the Exaflop Era, San Jose, California, June 5, 2011. **Keynote.**

“Center Challenges 2021,” Panel on New Challenges in the Next Decade, SciDAC PI Meeting, Denver, Colorado, July 2011. **Invited Panelist.**

“NERSC Role in Nuclear Physics Research,” ASCR/NP NERSC Requirements Workshop, Bethesda, Maryland, May 2011.

“Exascale Computing: More and Moore?” ACM International Conference on Computing Frontiers, Ischia, Italy, May 4, 2011. **Keynote.**

“Exascale Computing: More and Moore?” University of Southern California (USC), Ming Hsieh Department of Electrical Engineering, Los Angeles, California, April 6, 2011. **Distinguished Lecture Series.**

“The Future of Computing Performance,” Department of Energy, Office of Science, Advanced Scientific Computing Advisory Committee (ASCAC), Washington, D.C., March 22, 2011.

“Programming Model Challenges,” National Research Council Symposium on Computing Performance, Washington, D.C., March 22, 2011.

“Exascale Technical Challenges,” American Chemical Society Congressional Briefing on Supercomputing for Science and Competitiveness, Washington, D.C., March 17, 2011.

“Hardware and Software Trends in Computational Systems for Biology,” Joint Genome Institute Users Meeting, Walnut Creek, California, March 2011.

“Exascale Computing: More and Moore?” International Center for Computational Science Workshop on Manycore and Accelerator-based High-performance Scientific Computing, Berkeley, California, March 2011. **Keynote.**

“Software and Algorithms for Exascale: Ten Ways to Waste and Exascale Computer,” Oil and Gas High Performance Computing Workshop, Rice University, Houston, Texas, March 3, 2011. **Invited talk.**

“NERSC Role in Advanced Scientific Computing Research,” ASCR NERSC Requirements Workshop, Oakland, California, January 2011.

“Saving the World with Computing (and Other Reasons to Study Computer Science),” guest lecture in CS10, “The Joy and Beauty of Computing” course in Fall 2010 at UC Berkeley.

“Toward Exascale Computing with Heterogeneous Architecture” Invited panel speaker at SC10 (“Supercomputing”), New Orleans, LA, November 16, 2010.

“Partitioned Global Address Space (PGAS)” Birds-of-a-Feathers session at SC10, New Orleans, November 16, 2010.

“Science in the Clouds,” Workshop on Petascale Data Analytics on Clouds: Trends, Challenges, and Opportunities, at SC10 (“Supercomputing”), November 14, 2010. **Invited talk.**

“Introduction to PGAS (UPC and CAF) and Hybrid for Multicore Programming.” Joint tutorial with Alice E. Koniges, Rolf Rabenseifner, Reinhold Bader, David Eder, SC10 (“Supercomputing”), November 14, 2010, New Orleans, LA.

“Exascale Computing: More and Moore?” MIT EECS Dertouzos Distinguished Lecture Series, Massachusetts Institute of Technology, Cambridge, MA, November 4, 2010. **Distinguished Lecture Invited Talk.**

“Science in the Clouds: A View from Berkeley,” ISC Cloud ’10, Frankfurt, Germany, October 29, 2010. **Keynote.**

“Cloud Debate: Cloud or Not Cloud, That is the Question,” ISC Cloud ’10, Frankfurt, Germany, October 28, 2010. Invited Panelist.

“NERSC Overview and Plans,” NERSC User Group Meeting. Oakland, CA, October 21, 2010.

“How can the partitioned global address space model be relevant to mainstream computing?” Partitioned Global Address Space Conference, October 17, 2010. Invited panel speaker.

“Paving the Road to Exascale,” International Conference on Parallel Programming (ICPP), September 16, 2010, San Diego, CA. **Keynote.**

“Support for Hierarchical Machines” UPCRC workshop, Redmond WA, August 12-13, 2010.

“NERSC Overview and Strategic Directions” Department of Energy, Office of Advanced Scientific Computing Research, August 2010.

“RAMP for Exascale”, RAMP Wrap, Stanford, CA, August 2010.

“NERSC Role in Fusion Energy Research Research,” FES Requirements Workshop for NERSC, Washington DC, August 2010.

“Bringing Users Along the Road to Billion Way Concurrency,” SciDAC PI Meeting, Chattanooga, TN, July 15, 2010. **Invited Talk.**

“Saving the World with Computing (and Other Reasons to Study Computer Science,” Workshop on Computer Science for High School Teachers, Berkeley, CA, June 2010. (Also given to Bay Area high school students at LBNL.)

“Autotuning: Past, Present and Future”, ParLab Retreat, June 2010, Tahoe City, CA.

“Energy Efficiency at Extreme Scales,” Santa Barbara Energy Efficiency Summit, May 12, 2010, Santa Barbara, CA. **Invited Talk.**

“Programming Models and Communication Libraries,” The Global Arrays Technical Meeting, May 6-7, 2010, Seattle, Washington. **Invited Talk.**

“Programming 100,000 Processors,” 16th Meeting of the IBM HPC Systems Scientific Computing User Group (SciCOMP/SPXXL), San Francisco, CA, May 11, 2010. **Invited Talk.**

“Programming Models from Petascale to Exascale,” University of Washington, Computer Science Department, Seattle, WA, May 7, 2010. **Invited talk.**

“DOE Exascale Initiative Technical RoadMap,” DOE Architectures and Technology Workshop, San Diego, CA, December 8, 2009.

“Scientific Computing with Accelerators: What, Why and How?” Workshop on Manycore and Accelerator-based Computing for Physics and Astronomy Applications. SLAC National Accelerator Laboratory/ Lawrence Berkeley National Laboratory, Stanford, CA, USA, November 30, 2009. **Keynote.**

“Beyond UPC”, Workshop on User Experience and Advances in Bridging Multicore's Programmability Gap at SC09 (“Supercomputing”), November 16, 2009. **Invited talk.**

“Programming Models from Petascale to Exascale,” UCLA Computer Science Department Distinguished Lecture Series, UCLA, November 12, 2009. **Invited talk.**

“NERSC Role in High Energy Physics Research,” HEP Requirements Workshop for NERSC, Washington DC, November 2009.

“NERSC Overview and Plans,” NERSC User Group Meeting, Boulder, Colorado, October 7-8, 2009.

“Beyond UPC”, 3rd Annual Conference on Partitioned Global Address Space (PGAS) Programming Models, Ashburn, Virginia, October 5-8, 2009. **Invited keynote.**

“Hardware and Software in the Multicore Era,” HEPiX Meeting, Berkeley California, October 26, 2009.

“Unified Parallel C (UPC)”, Programming Models for Multicore, Lausanne Switzerland, September 7, 2009.

Invited talk.

“HPC Trends in Software,” International Computational Accelerator Physics Conference (ICAP’09), San Francisco, California, September 2009. **Invited talk.**

“Multicore Meets Exascale: Catalyst for a Software Revolution,” NVIDIA, July 2009. **Invited talk.**

“An Approach to Productivity,” ParLab Retreat, Santa Cruz, California, June 2009.

“Multicore/Manycore: What Can We Expect from the Software?” International Conference on Supercomputing (ICS’09), Hamburg, Germany, June 2009. **Invited talk.**

“The Role of Compilers in Manycore Programming,” University of Illinois at Urbana-Champaign, February 2009.

“Ten Ways to Waste a Parallel Computer,” International Symposium on Computer Architecture (ISCA’09), June 22, 2009. **Invited keynote.**

“Multicore/Manycore: What can we Expect from Software?” International Supercomputing Conference, Hamburg Germany, June 25, 2009, **Invited Talk.**

“NERSC Role in Biological and Environmental Research,” BER Requirements Workshop for NERSC, Washington DC, May 2009.

“Center for Scalable Application Development Software (CScADS): Libraries and Compilers,” CScADS Review, April 2009.

“Programming Models for Manycore,” University of British Columbia **Distinguished Lecture Series**, Vancouver, Canada, February 2009.

“The Role of Compilers in Manycore Programming,” University of Illinois at Urbana Champagne (UIUC) Workshop, February 2009.

“Overview of the PGAS Programming Model and the Berkeley UPC Project,” UPC Project Review, Berkeley, CA, February 2009.

“Programming Model Challenges for Managing Massive Concurrency,” Workshop, Supercomputing 2008 (SC08), Austin TX, November 2008.

“To Virtualize or Not to Virtualize,” Workshop, Supercomputing 2008 (SC08), Austin TX, November 2008.

“Compiler and Runtime Issues at Exascale,” Exascale Birds-of-a-Feather Session (BoF), Supercomputing 2008 (SC08), Austin TX, November 2008.

“Titanium Overview,” Partitioned Global Address Space (PGAS) Birds-of-a-Features Sesssion (BoF), Supercomputing 2008 (SC08), Austin TX, November 2008.

“Programming Models for Parallel Machines,” UCB Bootcamp on Parallel Computing, Berkeley, California, August 25-36, 2008.

“Multicore: Fallout from a Hardware Revolution,” South Dakota School of Mining and Technology, Rapid City, South Dakota, September 24, 2008. **Invited talk.**

“Scheduling UPC Threads on GPUs and Multicore,” UPC Developers Workshop, Washington, DC, September 22-23, 2008.

“Programming Models for Manycore Processors,” Intel UPCRC Programming Languages Workshop, August 23, 2008, Santa Clara, CA.

“PERI, Tuning for Multicore,” SciDAC PI Meeting, Seattle, WA, July 14-17, 2008. (Filling in for scheduled speaker Sam Williams. **Invited talk.**)

“Programming Models: Opportunities and Challenges for Scalable Applications,” Next Generation Scalable Applications: When MPI Only is Not Enough. June 3-5, 2008.

“Programming Models for Manycore Systems,” Intel Corp., Santa Clara, CA, April 23, 2008. **Keynote.**

“Multicore Meets Exascale: The Catalyst for a Software Revolution,” 2008 Salishan Conference on High Speed Computing, Salishan, OR, April 21-22, 2008. **Keynote.**

“Programming Models for Petascale to Exascale,” IPDPS 2008, Miami, FL, April 15-16, 2008. **Keynote.**

“Programming Models for Petascale,” North Carolina State University, Raleigh, NC, Feb 10-12, 2008. Research Triangle **Distinguished Lecture Series**, Invited Talk.

“Multicore Meets Petascale: The Catalyst for a Software Revolution,” Princeton University, Princeton, NJ, February 25-26, 2008. Invited Talk.

“Programming Techniques to Harness Exaflops,” Frontiers of Extreme Scale Computing: From Nanoscale to Zettascale, Santa Cruz, California. October 21-25, 2007.

“Programming Model Issues in Petascale Computing,” Symposium on Turbulence & Dynamios at Petaspeed Boulder, Colorado, October 15-19, 2007.

“Productivity and Performance using Partitioned Global Address Space Languages,” Parallel Symbolic Computation (PASCO '07), London, Canada, July 27-28, 2007. Invited talk.

“Partitioned Global Address Space Languages for Multilevel Parallelism,” Center for Scalable Application Development Systems (CScADS) Workshop on Petascale Architectures. Snowbird, Utah, July 23-26, 2007. Invited talk.

“Automatic Performance Tuning Workshop,” Center for Scalable Application Development Systems (CScADS) Workshop on Automatic Performance Tuning. Snowbird, Utah, July 9-12, 2007. (Overview talk as program co-chair.)

“Partitioned Global Address Space Languages for Multilevel Parallelism,” Petascale Applications Symposium: Multilevel Parallelism and Locality-Aware Algorithms Pittsburgh Supercomputing Center, Pittsburgh, Pennsylvania, June 22-23, 2007. Invited talk.

“Tools and Libraries for Manycore Computing,” Manycore Computing Workshop, Seattle, Washington, June 20-21, 2007. Invited panel speaker.

“Parallel Languages: Past, Present and Future,” History of Programming Languages (HOPL-III), San Diego, California, June 9-10, 2007. Invited panel speaker.

“The Tenure Process,” CRA-W Career Mentoring Workshop, San Diego, California, June 9-10, 2007. Sponsored by the Computer Research Association's Committee on the Status of Women in Computing Research (CRA-W). Invited panel speaker.

“How to Write a Bad Proposal,” CRA-W Career Mentoring Workshop, San Diego, California, June 9-10, 2007. Sponsored by the Computer Research Association's Committee on the Status of Women in Computing Research (CRA-W). Invited panel speaker.

“The Berkeley View: Applications-Driven Research in Parallel Programming Models and Architectures,” Multicore-the New Face of Computing-Promises and Challenges, 8th IEEE/NATEA Annual Conference on New Frontiers in Computing Technology, June 2, 2007, Stanford University. **Keynote.**

“Compilation Techniques for PGAS Languages,” 5th Annual Workshop on Charm++ and its Applications, Parallel Programming Lab, University of Illinois at Urbana-Champaign April 18th-20th, 2007. **Keynote.**

“Architectural Trends and Programming Model Strategies for Large-Scale Machines,” MSRI Symposium on Climate Change, "From Global Models to Local Action." April 11-13, 2007. Invited talk.

“Overview of Titanium and the HPLS Program,” The Second Geoscience Application Requirements for Petascale Architectures, Feb 21-22, 2007, San Diego, California. Invited talk.

“Programming Models for Parallel Computing,” Interactive Parallel Computation in Support of Research in Algebra, Geometry and Number Theory, Berkeley, California, January 29-February 2, 2007. Invited talk.

“Compilation Techniques for Partitioned Global Address Space Languages,” The 19th International Workshop on Languages and Compilers for Parallel Computing, New Orleans, Louisiana, November 2-4, 2006. **Keynote.**

“Performance Advantages of Partitioned Global Address Space Languages,” EuroPVM/MPI '06, Bonn, Germany, September 17-20, 2006. Invited talk.

“Use of a high-level language in high performance biomechanics simulations.” Abstract appeared in the Journal of Biomechanics, “Abstracts of the 5th World Congress on Biomechanics,” July 29-August 4, 2006, Munich, Germany, p. S435.

“Optimizations for Partitioned Global Address Space Languages,” Thirteenth AURORA Plenary Meeting, Workshop on High Productivity Programming Language Systems, Strobl/Wolfgangsee, Austria, June 9-11, 2006. Invited talk.

“Using Meshes, Matrices, and Particles in Partitioned Global Address Space (PGAS) Languages,” Scientific Discovery through Advanced Computing (SciDAC), Denver, Colorado, June 25-29, 2006. Invited talk.

“Performance and Productivity Opportunities Using Global Address Space Programming Models,” PetaScale Computation for the Geosciences Workshop, San Diego Supercomputing Center, April 5, 2006.

“Using High Level Languages in Computational Frameworks,” Computational Frameworks (CompFrame) '05, Atlanta, Georgia, June 22-23, 2005. Invited talk.

“Finding a Research Topic,” CRA-W Graduate Cohort Program, San Francisco, California, February 25-26, 2005.

“Towards a Digital Human: Scalable Simulation of the Heart and Other Organs,” EECS Joint Colloquium Distinguished Lecture Series, University of California at Berkeley, September 15, 2004. Invited talk.

“Towards a Digital Human: Simulation of the Heart and Other Organs,” Distinguished Lecture Series, University of California at Davis, April 2004. Invited talk.

“Programmability, Performance, and Portability of Global Address Space Languages,” High Performance Computing User Forum, Tucson, Arizona, September 21-22, 2004. Invited talk.

“Report on High-End Computing Research and Development in Japan,” Meeting of the Coalition for Academic Scientific Computation, July 14-15, 2004. Invited talk.

“Latency vs. Bandwidth: Which Matters More?” Workshop on Software for Processor-In-Memory Based Parallel Systems, at the Second Annual IEEE/ACM International Symposium on Code Generation and Optimization, San Jose, California, March 21, 2004. Invited talk.

“High Performance Programming in the Partitioned Global Address Space Model,” Short course co-taught with Tarek El-Ghazawi and Robert Numrich at the SIAM Conference on Parallel Processing for Scientific Computing, San Francisco, February 25-27, 2004.

“Titanium: A Java Dialect for High Performance Computing,” given as part of a tutorial on "UPC, Co-Array Fortran, and Titanium: Programming with the Partitioned Global Address Space Model." Supercomputing (SC03), November, 2003.

“Optimizing Java-Like Languages for Parallel and Distributed Environments,” Programming Language Design and Implementation, June 2001. Invited tutorial.

“Language and Compiler Support for Adaptive Mesh Refinement,” Caltech, Spring 2000. Invited talk.

“Exploiting On-Chip Memory Bandwidth in the VIRAM Compiler,” 2nd Workshop on Intelligent Memory Systems. In conjunction with Architectural Support for Programming Languages and Operating Systems, Boston Massachusetts, November 12, 2000.

“System Support for Data-Intensive Applications,” University of Washington, CRAW-Lucent Invited Lecture, Spring 2000.

“Titanium: A High Performance Java Dialect,” SIAM Conference on Parallel Processing for Scientific Computing, 1999.

“Compiling Explicitly Parallel Programs,” SIAM conference on Parallel Processing for Scientific Computing, 1997.

“Systems Support for Irregular Parallel Applications,” Irregular '96, Santa Barbara, California, August 19-21, 1996. Invited talk.

Co-authored Posters and Presentations

Eun-Jin Im, Cleve Ashcraft, Ismail Bustany, Katherine Yelick, “A Computationally Efficient Triple Matrix Product for a Class of Sparse Schur-Complement Matrices,” SIAM Conference on Parallel Processing for Scientific Computing. San Francisco, California, February 2004.

Dan Bonachea, Rajesh Nishtala, Paul Hargrove, Mike Welcome, Katherin Yelick, “Optimized Collectives for PGAS Languages with One-Sided Communication,” Supercomputing (SC06), November 2006

Dan Bonachea, Rajesh Nishtala, Paul Hargrove, Katherine Yelick, “Efficient Point-to-Point Synchronization in UPC,” 2nd Conf. on Partitioned Global Address Space Programming Models ([PGAS06](#)), October 2006

Dan O Bonachea, Christian Bell, Rajesh Nishtala, Kaushik Datta, Parry Husbands, Paul Hargrove, Katherine Yelick, “The Performance and Productivity Benefits of Global Address Space Languages,” Supercomputing, November 2005.

Rajesh Nishtala, Richard Vuduc, James Demmel, and Katherine Yelick, “When Cache Blocking Sparse Matrix Multiply Works and Why.” PARA'04 Workshop on State-of-the-art in Scientific Computing, Copenhagen, Denmark, June 2004.

E.-J. Im, I. Bustany, C. Ashcraft, J. Demmel, K. Yelick, “Toward automatic performance tuning of matrix triple products based on matrix structure.” PARA'04 Workshop on State-of-the-art in Scientific Computing, Lyngby, Denmark, June 20-23, 2004. Full paper in Applied Parallel Computing: State of the Art in Scientific Computing. Lecture Notes in Computer Science, 2006, Volume 3732/2006, 740-746, DOI: 10.1007/11558958_89. Revised Selected Papers from PARA 2004, Jack Dongarra, Kaj Madsen, Jerzy Wasniewski (Eds.): Springer 2006, ISBN 3-540-29067-2.

Advising

Postdoctoral Researchers

Greg Balls, computational fluid dynamics in Titanium, 2001.

Eun-Jin Im, autotuning of sparse matrix kernels, 2000-2001.

Ed Givelberg, an immersed boundary method framework in Titanium, used for simulating the inner ear, 2002-2005.

Karl Fuerlinger, performance tools for parallel machines, 2008-2010.

PhD Students

- Shoaib Kamil. Thesis topic: "SEJITS: Bringing Parallel Performance to Productivity Languages," PhD expected May 2011.
- Amir Kamil. Thesis topic: "Hierarchical Additions to the SPMD Programming Model," expected May 2011.
- Jimmy Su. PhD thesis title: "Optimizing Irregular Data Accesses for Cluster and Multicore Architectures," December 2010.
- Kaushik Datta. PhD thesis title: "Auto-tuning Stencil Codes for Cache-Based Multicore Platforms." December 2009.
- Rajesh Nishtala. PhD thesis title: "Automatically Tuning Collective Communication for One-Sided Programming Models," December 2009.
- Wei Chen. PhD thesis title, "Optimizing Partitioned Global Address Space Programs for Cluster Architectures," August 2007.
- Eun-Jin Im, PhD thesis title, "Optimizing the Performance of Sparse Matrix-Vector Multiplication," May 2000.
- Deborah Weisser. PhD thesis title, "Interacting Agents for Local Search," May 1999.
- Arvind Krishnamurthy. PhD thesis title, "Compiler Analyses and System Support for Optimizing Shared Address Space Programs," December 1998.
- Soumen Chakrabarti. PhD thesis title, "Efficient Resource Scheduling in Multiprocessors," June 1996.
- Chih-Po Wen. PhD thesis title, "Portable Library Support for Irregular Applications," December 1995.

Master's Students

- Brian Kazian, "Performance Study for Contributing Area Estimation in Parallel with UPC," December 2009.
- Jason Duell, Master's report, "Pthreads or Processes: Which is Better for Implementing Global Address Space languages?" June 2007.
- Rajesh Nishtala. Master's report title, "Architectural Probes for Measuring Communication Overlap Potential," May 2006.
- Amir Kamil. Master's report title, "Analysis of Partitioned Global Address Space Programs," December 2006.
- Kaushik Datta. Master's report title, "The NAS Parallel Benchmarks in Titanium," December 2005.
- Jimmy Su. Master's report title, "Automatic Support for Irregular Computations in a High Level Languages," May 2005.
- Christian Bell, "Design and Implementation of a Distributed Memory DMA Registration Strategy for Pinning-based High Performance Networks," May 2005.
- Wei Chen. Master's report, "Building a Source to Source UPC Translator," December 2004.
- Siu Man Yau, "Experiences in Using Titanium for Simulation of Immersed Boundary Biological Systems," May 2002.
- Dan Bonachea. Master's report title, "Bulk File I/O Extensions to Java," May 2000.
- Noah Treuhaft. "Enhancing Graduated Declustering for Better Performance Availability on Clusters," December 2000.
- Chang-Sun Lin Master's report title, "The Performance Limitations of SPMD Programs on Clusters of Multiprocessors," May 2000.
- Elaine Randi Thomas. Master's Report title, "An Architectural Performance Study of the Fast Fourier Transform on Vector IRAM," May 2000.

- Ngeci Bowman. ``Random Projection: A Data Compression Algorithm for EM" December 1999.
- Arvind Krishnamurthy. Master's report, "Compiling Explicitly Parallel Programs," May 1994.
- Steve Steinberg. Master's report, "Parallelizing a Cell Simulation: Analysis, Abstraction, and Portability," December 1994.
- Ruth Hinkins. Master's report, "Parallel Computation of Automatic Differentiation Applied to Magnetic Field Calculations," September 1994.
- Jeff Jones. Master's report, "Parallelizing the Phylogeny Problem," December 1994.
- Soumen Charkrabarti. Master's report, "Computing Grobner Bases on a Distributed Memory Multiprocessor," December 1992.
- Chih-Po Wen. Master's report, "Timing Simulation on Distributed Memory Multiprocessor," December 1992.

Undergraduate Research Students

Ankit Jain, 2005-2007

Wei Tu, 2004

Benjamin Lee, 2002-2004

Omair Kamil, 2004

Meling Ng, 2004

Siu Man Yau, 1999.

Kar Ming Tang, 1999.

Eric Reeber, 1999.

Glen Jeh, 1999.

Stanley H. Yue, 1999.

Andy Hung Ng, 1999

Sumeet Shendrikar, 1999

Anthony Lai, 1999.

Steve Benting, 1997-1998.

Karl Czajkowski, 1995-1996.

Daniel Yu, 1996.

Ronald Yong, 1996.

David Yan, 1996.

Jun Yang, 1995-1996.

Jenny Ng, 1994.

Boon-Yuen Ng, 1994.

Eric Liu, 1994.

Matthew Thorn, 1994.

Kevin Gong, 1992.

Dindo Siasoyco, 1992.

Research and Facility Funding

Project: National Energy Research Scientific Computing (NERSC) Center

Investigators: Katherine Yelick (PI)

Source of Support: DOE

Location of Project: Lawrence Berkeley National Laboratory

Duration: 10/1/2010-9/30/2011 (annual appropriation, which is a Congressional line item)

Total FY11 Funding: \$57,800,000

Project: Center for Programming Models for Scalable Parallel Computing

Investigators: Katherine Yelick (PI)

Source of Support: DOE

Location of Project: U.C. Berkeley

Duration: 9/15/06-9/14/2011

Total Funding: \$2,116,480

Project: Center for Scalable-Performance Application Development Software

Investigators: Katherine Yelick (UCB PI), John Mellor-Crummey (Coordinating PI at Rice)

Source of Support: DOE

Location of Project: U.C. Berkeley

Duration: 11/15/2006-11/14/2011

Total Funding: \$675,000

Project: CRI:IAD: Development of a Research Infrastructure for the Multithreaded Computing Community Using the Cray Eldorado Platform

Investigators: Katherine Yelick (UCB PI), Jay Brockman (Lead PI at Notre Dame)

Source of Support: NSF

Location of Project: U.C. Berkeley

Duration: 8/1/2007-7/1/2012

Total Funding: \$50,000

Project: SDCI: IPM – a Performance Monitoring Environment for Petascale HPC
Investigators: Katherine Yelick (UCB PI), Allan Snaveley (Lead PI at UCSD)
Source of Support: NSF
Location of Project: U.C. Berkeley
Duration: 10/01/2007-9/30/2011
Total funding: \$753,357

Project: PetaApps: New Coupling Strategies and Capabilities for Petascale Climate Modeling
Investigators: William Collins (UCB PI), Katherine Yelick (co-PI), Jim Kinter (Coordinating PI, COLA), and others
Source of Support: NSF
Location of Project: UC Berkeley
Duration: 3/01/2008-2/28/12
Total funding: \$391,130

Project: Parallel Laboratory
Investigators: David Patterson (PI), Ras Bodik (co-PI), James Demmel (co-PI), Kurt Keutzer (co-PI), Koushik Sen (co-PI), Kathy Yelick (co-PI), Krste Asanovic (co-PI)
Source of Support: Intel and Microsoft
Location of Project: UC. Berkeley
Duration: 12/31/07-12/30/12
Total Funding: \$6,000,000

Project: Parallel Laboratory
Investigators: David Patterson (PI), Ras Bodik (co-PI), James Demmel (co-PI), Kurt Keutzer (co-PI), Koushik Sen (co-PI), Kathy Yelick (co-PI), Krste Asanovic (co-PI)
Source of Support: UC Discovery Funds
Location of Project: UC. Berkeley
Duration: 5/01/08-4/30/12
Total Funding: \$2,125,000

Project: Unified Parallel C
Investigators: K. Yelick (PI), C. Iancu (co-pI)
Source: Department of Defense
Amount: \$1,343,000 (including subcontracts)
Location of Project: LBNL
Period: April 1, 2010 – September 30, 2011

Project: Unified Parallel C on Scalable Shared Memory
Investigators: K. Yelick (PI)
Source: Department of Defense
Amount: \$1,002,663 (including subcontracts)
Location of Project: LBNL
Period: July 28, 2010 – September 30, 2011

Project: Applications and Runtime Systems Using Fast One-Sided Communication
Investigators: Katherine Yelick
Source of Support: DOE
Annual Amount: \$530,000
Location of Project: LBNL
Period: October 1, 2010 – September 30, 2011